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ORIGINAL RESEARCH

A five-level nested neutral point-clamped inverter topology

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Abstract

Classical five-level nested neutral point-clamped (5L NNPC) inverter-leg is a hybrid of the flying-capacitor and diode-clamped 5-L inverter-leg configurations. Though uniform reduced voltage stress on the constituting switches is evident in 5L NNPC inverter-leg, trails of the drawbacks of diode-clamping concept still exist. Compared with the classical 5L NNPC inverter, the state-of-the-art diode-free 5L NNPC inverter involves no passive power switches and has low conduction losses. However, in this 5L NNPC inverter, two of the eight active switches have blocking voltage rating of 1/2 of the input voltage. Considering this limiting topological feature, an inverter-leg for 5L NNPC inverter is presented in this paper. In the proposed 5L NNPC inverter-leg, only one switch has voltage stress of 1/2 of the input voltage. This reduced voltage stress has inverter cost and loss implications. The performances and competitiveness of the 5L NNPC inverter were analysed in detail and demonstrated with a prototype. The blocking voltages of all the constituting power switches; profiles of the flying-capacitor voltages; and FFT spectrum of line voltage waveform were experimentally obtained. Experimental deactivation and activation of the inverter's capacitor voltages balancing scheme were typified for varying modulation index values.

1 | INTRODUCTION

Classical single-source multilevel inverter (SSMLI) topological features, controls and applications have been well documented in the literature [1–7]. Even though that these conventional SSMLIs with output voltage levels beyond 3 still maintain uniform reduced voltage stress on the constituting power devices, such configurations have inherent pronounced drawback of excessive number of power circuit component-count. The need for higher output voltage levels is justified in view of the overall power-conditioning system's operating voltage magnitude and inverters' output voltage quality. In response to this need, five-level MLI power circuit configurations that depict certain improved topological features have been reported in the literature [8–13].

In [8], the input voltage source was split by 4 capacitor banks with 3 mid-points. In each phase, 3 bidirectional switches were used to clamp these mid-points to the corresponding output phase node. The inverter has undue varying voltage stresses on the constituting power switches; and besides, voltage balancing circuit is needed. Modification of the circuit in [8] is seen in [9]; therein, only one bidirectional switch has been used; but undue varying voltage stresses on the switches is still retained.

Two input voltage splitting capacitor banks and one flying capacitor were deployed in configuring a five-level active neutral-point clamped, 5L ANPC, inverter-leg in [10]. This inverter-leg has 4 of its 8 active power switches rated at half of the dc-link voltage. Rest of the switches has one-fourth dc-link blocking voltage rating. Improved topology of the 5L ANPC inverter-leg was presented in [11]. Space vector pulse-width modulation (SVPWM) and sinusoidal pulse-width modulation (SPWM) control schemes have been developed for the 5L ANPC inverter [12–15].

[16] presented the topology and control of a five-level nested neutral-point clamped (5L NNPC) inverter. Less number of flying-capacitors and clamping diodes were nested in each inverter-leg alongside the supposed eight active power switches as shown in Figure 1a. A more compact configuration for the 5L NNPC inverter-leg was presented in [17]; as shown in Figure 1b. The passive clamping diodes in Figure 1a were removed, but the 1/4 dc-link reverse blocking voltage rating of 2 switches

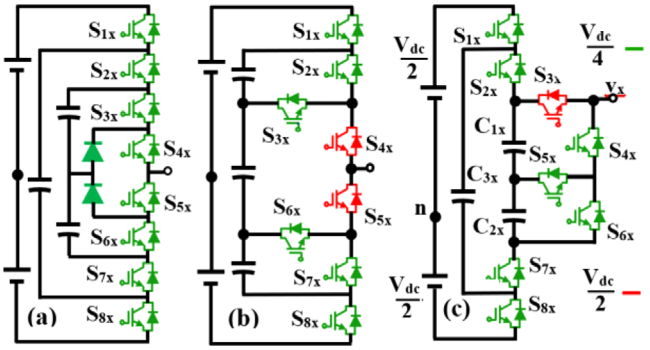

FIGURE 1 5L NNPC inverter-legs in (a) [16], (b) [17], (c) proposed.

in Figure 1a is compromised to half dc-link reverse blocking voltage rating in Figure 1b.

In Figure 1b, two switches have half dc-link reverse blocking voltage rating. The possibility of reducing this number presents itself in the power circuit proposed in this paper; shown in Figure 1c. In this 5L inverter inverter-leg, only one power switch has half dc-link reverse blocking voltage rating; while the rest of the switches retain the 1/4 dc-link voltage stress rating. This innate topological feature of the proposed inverter-leg reflects in reduced loss and cost involvement when viewed alongside power circuits in Figure 1a,b.

In the following sections, power circuit configuration and operation of the proposed inverter will be presented in Section 2. Also in this section, effects of the inverter switching states on capacitor voltages will be detailed. The sinusoidal pulse-width modulation, SPWM, Scheme that entrenches smooth operation of the inverter is presented in Section 3. Exploration of the cost and loss involvements of the inverter configuration in relation to classical and recent 5L, NNPC inverter power circuits were done in Section 4. Validations of the inverter performances were done via simulation and experimental studies in Section 5.

2 | PROPOSED 3-PHASE 5L NNPC INVERTER TOPOLOGY

Based on the topological feature of the proposed inverter-leg, a switching scheme is developed for the synthesis of all the inverter voltage levels. Presence of redundant switching states facilitates the formulation of the appropriate capacitor voltage balancing scheme for this inverter topology; such scheme is based on the effects of the switching states on the nested capacitor voltages.

2.1 | 3-phase, 5L ANNPC inverter power circuit

A leg of the proposed 5L NNPC inverter is shown in Figure 1c. Relatively, it is a modification of the 5L NNPC inverter circuit in Figure 1a; whereby the 3L NPC sub-circuit (circled with dotted line) in Figure 1a has been reconfigured in view of achieving all-active-switch five-level inverter-leg; the clamping diodes have been removed. As in Figure 1a, the voltage across each of the 2 series flying-capacitors (C_{1x} and C_{2x}; x is the phase notations: a, b, c) is $V_{dc}/4$; where V_{dc} is the input dc-link. However, the trade-off is the increased $V_{dc}/2$ voltage stress of only one power switch, S_{3x}. Topologically, the proposed inverter-leg is equivalent to the power circuits in Figure 1a,b; and hence, it can generate five output voltages: $V_{dc}/2$, $V_{dc}/4$, 0, $-V_{dc}/4$, and $-V_{dc}/2$ with reference to the mid-point, n, of the input dc-link; arbitrarily tagged with corresponding positive integers: 0, 1, 2, 3, and 4 to depict the generated inverter-leg output voltage level, L_x. The possible 4-switch combinations of the power switches that synthesize these inverter-leg output voltages, v_{xn}, are given in Table 1. The 4 pairs of switches are complementary: $S_{8x} = \overline{S_{1x}}$, $S_{7x} = \overline{S_{2x}}$, $S_{4x} = \overline{S_{3x}}$, and $S_{6x} = \overline{S_{5x}}$. The synthesis of $-V_{dc}/4$ or $V_{dc}/4$ involves three redundant switching combinations; that of zero voltage level involves four redundant switching combinations; whereas only one switching combination exists for either generation of $-V_{dc}/2$ or $V_{dc}/2$. This existence and non-existence of redundant switching states, RS_x, in the inverter-leg output voltage level, L_x, is reflected in the last column of Table 1; where the letters A, B, C, and D are used to denote the redundant switching states in output voltage levels 1, 2, and 3. It is obvious from Table 1 and Figure 1c that it is only switch S_{3x} that has maximum blocking voltage of $V_{dc}/2$; the rest of the switches have maximum blocking voltage of $V_{dc}/4$ each. The three-phase power circuit of the 5L ANNPC inverter is shown in Figure 2.

TABLE 1 Switching states and corresponding synthesized output voltages of the 5L ANNPC Inverter-Leg.

Switching state combinations										
S_{1x}	S_{2x}	S_{3x}	S_{4x}	S_{5x}	S_{6x}	S_{7x}	S_{8x}	V_{xn}	L_x	RS_x
1	1	1	0	1	0	0	0	$0.5V_{dc}$	4	4
1	1	0	1	1	0	0	0	$\frac{V_{dc}}{4}$	3	3C
0	1	1	0	1	0	0	1			3B
1	0	1	0	1	0	1	0			3A
1	1	0	1	0	1	0	0	0	2	2D
1	0	0	1	1	0	1	0			2C
0	1	0	1	1	0	0	1			2B
0	0	1	0	1	0	1	1			2A
0	0	0	1	1	0	1	1	$-\frac{V_{dc}}{4}$	1	1C
1	0	0	1	0	1	1	0			1B
0	1	0	1	0	1	0	1			1A
0	0	0	1	0	1	1	1	$-0.5V_{dc}$	0	0

2.2 | Effects of the switching states on capacitor voltages

In Table 1, the possible on/off switching state combinations in each of the 5L NNPC inverter-leg are given. Each of the 12-row

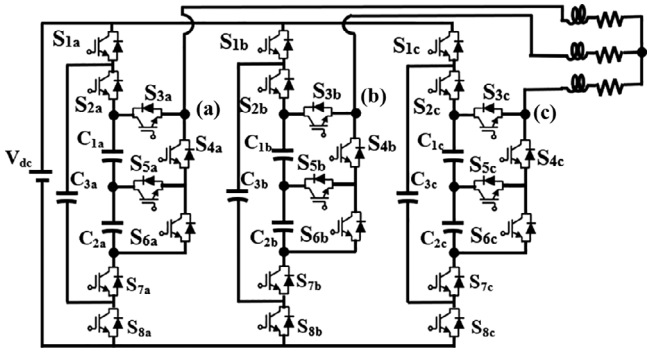

FIGURE 2 Proposed 3-phase, 5L NNPC inverter power circuit.

switch combinations has varying effect on the voltage status of the 3 nested capacitor voltages (v_{C1x}, v_{C2x}, v_{C3x}); depending on the direction of the corresponding phase current, i_x. Current flow out of inverter-leg output node is considered positive (>0) and negative (<0) otherwise.

The synthesis of voltage level $-V_{dc}/4$ involves three redundant switching states; RS_x equals 1A, 1B, and 1C corresponding to rows 11, 10, and 9 in Table 1. Operational status of state 1A can be explained by considering the direction of the current, i_x. For positive direction of i_x, C_{3x} is discharged (v_{C3x} decreases) and both C_{1x}, C_{2x} are charged (v_{C1x}, v_{C2x} increase); for i_x negative, C_{3x} is charged and C_{1x}, C_{2x} are discharged. Operational status explanations for states 1B and 1C follow suit. Generation of zero voltage level involves four redundant switching states 2A, 2B, 2C, and 2D; corresponding to rows 8, 7, 6, and 5 in Table 1. As an example, operational status of state 2B is explained as follows: positive i_x charges C_{1x} and discharges C_{3x}; the reverse is the case for negative i_x; both positive and negative flow of i_x have no effect on capacitor C_{2x} voltage. States 2A, 2C and 2D status can be explained in similar way. Three redundant switching states 3A, 3B, and 3C are at disposal for obtaining voltage level $V_{dc}/4$; as depicted in Table 1. Considering operational status of state 3C, positive and negative directions of i_x have no effect on C_{2x} and C_{3x} voltages, but charges and discharges C_{1x}, respectively. Explanations of operational status of states 3A and 3B follow similarly. In Table 1, switching combinations corresponding to states 4 and 0 are indicated. For positive and negative flows of i_x, capacitors C_{1x}, C_{2x}, and C_{3x} are not involved in either of these current paths and hence their voltages, v_{C1x}, v_{C2x}, and v_{C3x}, are not affected. Table 2 summarizes these effects.

TABLE 2 Effects of switching states and Inverter-leg current on the flying-capacitor voltages.

				Effects on the capacitor voltages		
V_{xn}	L_x	RS_x	i_x	V_{C1x}	V_{C2x}	V_{C3x}
$0.5V_{dc}$	4	4	+	No effect	No effect	No effect
			−			
$\frac{V_{dc}}{4}$	3	3C	+	Charge	No effect	No effect
			−	Discharge	No effect	No effect
		3B	+	No effect	No effect	Discharge
			−	No effect	No effect	Charge
		3A	+	Discharge	Discharge	Charge
			−	Charge	Charge	Discharge
0	2	2D	+	Charge	Charge	No effect
			−	Discharge	Discharge	No effect
		2C	+	No effect	Discharge	Charge
			−	No effect	Charge	Discharge
		2B	+	Charge	No effect	Discharge
			−	Discharge	No effect	Charge
		2A	+	Discharge	Discharge	No effect
			−	Charge	Charge	No effect
$-\frac{V_{dc}}{4}$	1	1C	+	No effect	Discharge	No effect
			−	No effect	Charge	No effect
		1B	+	No effect	No effect	Charge
			−	No effect	No effect	Discharge
		1A	+	Charge	Charge	Discharge
			−	Discharge	Discharge	Charge
$-0.5V_{dc}$	0	0	+	No effect	No effect	No effect
			−			

3 | SINUSOIDAL PULSE-WIDTH MODULATION, SPWM, SCHEME FOR THE PROPOSED 5L ANNPC INVERTER

SPWM technique is deployed in the switching signals generation. The control approaches developed for the 5L NNPC inverter are well suited for the proposed 5L NNPC inverter. Thus, simplified SPWM control scheme in [16] is adopted to handle the flying-capacitors' voltage balancing in Figure 1c. For proper synthesis of the inverter-leg 5L staircase waveform, reference voltage values (v_{Cx1ref}, v_{Cx2ref}) for the flying-capacitors' voltages v_{C1x} and v_{C2x} should be $V_{dc}/4$; and $3V_{dc}/4$ for v_{C3x} (v_{Cx3ref}). In real operation, actual capacitors' voltages have the propensity of deviating significantly from these desired reference voltage values. The respective differences between the actual capacitors' voltages (v_{Cxi}; i = 1,2,3) and the reference voltages ($v_{Cxi,ref}$,) give the capacitor voltage deviations, Δv_{Cxi}:

$$\Delta v_{Cxi} = v_{Cxi} - v_{Cxi,\,ref} \tag{1}$$

In relation to the 'charge' and 'discharge' entries in Table 2,

$$\text{'charge'} = -\Delta v_{Cxi} \tag{2}$$

$$\text{'discharge'} = \Delta v_{Cxi} \tag{3}$$

Referring to Table 2, it can be seen that redundant states 1A, 1B, and 1C have dominant effects on capacitor C_{2x} and C_{3x} voltages; and hence these capacitors can be significantly con-

trolled within this level 1. Similar trend is evident in level 3 where redundant states 3A, 3B, and 3C have greater influences on capacitor C_{1x} and C_{3x} voltages. Thus, v_{C1x} and v_{C3x} are nicely controllable in level 3. Also, the four redundant states 2A, 2B, 2C, and 2D in level 2 have equal varying net influences on C_{1x}, C_{2x}, and C_{3x} voltages; these lead to v_{C1x}, v_{C2x}, and v_{C3x} having equal chances of being controlled in level 2. Proper generation of the voltage levels $V_{dc}/4$ demands guided-choice in choosing states 3A, 3B, and 3C; such prescribed choices are also needful in selecting states 2A, 2B, 2C, 2D and 1A, 1B, 1C in the syntheses of 0 and $-V_{dc}/4$ voltage levels, respectively. In level 1, the selection guideline is developed by considering C_{2x} and C_{3x} as 2 groups of capacitors alongside the states, 1A, 1B, 1C.

This grouping is facilitated by the inherent trend in Table 2. Irrespective of the direction of the inverter-leg current (i_x) in Table 2, states 1A and 1B always have reverse effect on v_{Cx3}; whereas states 1A and 1C always have reverse effect on v_{Cx2}. Thus, v_{Cx3} with states 1A and 1B is considered as a group; the other group is v_{Cx2} with states 1A and 1C. In the charging or discharging (redundant switch selection) of either group of capacitors, priority is given to the capacitor voltage whose absolute value is higher than the other. Now, substituting (from Equations (2) and (3)) Δv_{Cx3} and $-\Delta v_{Cx3}$ for 'discharge' and 'charge' in Table 2 and considering separately the effects on groups v_{Cx3} and v_{Cx2}, it can be deduced that: whenever $|\Delta v_{Cx3}| > |\Delta v_{Cx2}|$,

(i) and the product of $\pm\Delta v_{Cx3}$ and $\pm i_x$ turns out to be positive, state 1A should be selected to balance v_{Cx3}; that is: $\Delta v_{Cx3} * i_x$ or $-\Delta v_{Cx3} * -i_x$
(ii) and product of $\pm\Delta v_{Cx3}$ and $\pm i_x$ is negative, state 1B should be selected to balance v_{Cx3}; that is:
$-\Delta v_{Cx3} * i_x$ or $\Delta v_{Cx3} * -i_x$
If $|\Delta v_{Cx2}| > |\Delta v_{Cx3}|$,
(iii) and the product of $\pm\Delta v_{Cx2}$ and $\pm i_x$ turns out to be positive, state 1C should be selected to balance v_{Cx3}; that is: $\Delta v_{Cx2} * i_x$ or $-\Delta v_{Cx2} * -i_x$
(iv) and the product of $\pm\Delta v_{Cx2}$ and $\pm i_x$ is negative, state 1A should be selected to balance v_{Cx2}; that is
$-\Delta v_{Cx2} * i_x$ or $\Delta v_{Cx2} * -i_x$

Similarly, v_{Cx3} with states 3A, 3B and v_{Cx1} with states 3A, 3C are considered as 2 groups in output level 3. The selection prescriptions in level 2 follow a similar pattern just as outlined for level 1. In Table 2, it can be seen that states 2B and 2D have same effect on v_{Cx1}; such is the case of 2A and 2C on v_{Cx2}. It means that either of these equal-effect states can be used in the grouping. No matter the direction of i_x, states 2B and 2C always have reverse effect on v_{Cx3}; whereas states 2B/2D, 2A, and 2A/2C, 2D always have reverse effect on v_{Cx1} and v_{Cx2}, respectively. These capacitor voltages and the corresponding redundant states form three groups in level 2. Note that in selecting a group, priority should be given to the capacitor voltage whose absolute value is the highest among the 3 capacitor voltages. The selection prescriptions in level 2 follow a similar pattern just as outlined for level 1. These selection criteria are summarized in Table 3; therein, 'Max' is the sampled maximum

TABLE 3 Selection criteria for balancing v_{Cx1}, v_{Cx2}, and v_{Cx3}.

	Conditions		
L_x	$\Delta v_{Cx3} * i_x$	Voltage magnitude	RS_x
1	+	$\|\Delta v_{Cx3}\| > \|\Delta v_{Cx2}\|$	1A
	−		1B
2	+	$\|\Delta v_{Cx3}\| =$ Max	2B
	−		2C
3	+	$\|\Delta v_{Cx3}\| > \|\Delta v_{Cx1}\|$	3B
	−		3A
	$\Delta v_{Cx1} * i_x$	Voltage magnitude	
2	+	$\|\Delta v_{Cx1}\| =$ Max	2A
	−		2B/2D
3	+	$\|\Delta v_{Cx1}\| > \|\Delta v_{Cx3}\|$	3A
	−		3C
	$\Delta v_{Cx2} * i_x$	Voltage magnitude	
1	+	$\|\Delta v_{Cx2}\| > \|\Delta v_{Cx3}\|$	1C
	−		1A
2	+	$\|\Delta v_{Cx2}\| =$ Max	2A/2C
	−		2D

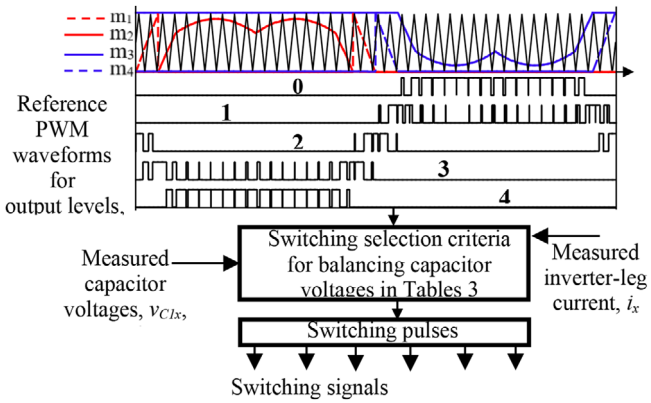

FIGURE 3 Control steps in each phase of the 5L NNPC inverter.

absolute voltage value between v_{Cx1}, v_{Cx2}, and v_{Cx3}. With these switching conditions, v_{Cx1}, v_{Cx2}, and v_{Cx3} are completely controllable irrespective of the direction of the inverter-leg current, i_x.

A commensurate single-carrier SPWM scheme, shown in Figure 3, is developed for the synthesis of the switches' gating signals. The reference PWM waveforms for output voltage levels, L_x, are generated by appropriate comparisons of modulating signals m_1, m_2, m_3, and m_4 with single triangular carrier, T. Zero-sequence component has been added to m_1, m_2, m_3, and m_4 in accordance to the min–max function principle; in view of extending the modulation index range beyond unity.

Control steps in each inverter-leg are depicted in this Figure 3.

TABLE 4 Cost comparison of 5L Inverter-Leg variants with Infineon semiconductor devices.

	In [16]		In [17]		Proposed	
Devices	**Qty**	**Price ($)**	**Qty**	**Price ($)**	**Qty**	**Price ($)**
FZ1200R17HE4 1700 V, 1200 A IGBT	8	5278	6	3958	7	4618
FZ1200R33HE3 3300 V, 1200 A IGBT	0	0	2	3346	1	1673
DD1200S17H4_B2 1700 V, 1200 A diode	2	1885	0	0	0	0
2ED300C17-S Gate driver	4	773	4	773	4	773
Cost summation		**7936**		**8077**		**7064**

4 | COST AND LOSS PERFORMANCES

To provide clues into the merits and drawbacks of the inverter-legs in Figure 1, comparisons among them are made based on their cost implications and loss performances. Same SPWM scheme and system parameters were used in all the inverter-leg variants. Parameters: 2.5 MVA rating; 6 kV input voltage; 3.3 kHz switching frequency; RL load (3.56 Ω, 2 mH).

4.1 | Inverter-legs cost evaluations and comparison

Arbitrarily, Infineon semiconductor power switch modules and gate drivers have been considered in the cost evaluations; based on the price list from Digi-key corporation in Poland (Ul. Krakowskie Przedmiescie 4/6, 00–333 Warsaw). The results are shown in Table 4.

The disparity in the cost of inverter-legs in Figure 1b,c is due to the reduced blocking voltage rating of one switch module in the proposed 5L inverter. On the other hand, the additional cost of 2 diodes significantly out-weighs the effect of reduced costs of low-voltage-rated switches in Figure 1a.

4.2 | Inverter-legs cost evaluations and comparison

PSIM simulation package was deplored in the computations of power losses in the power switches. PSIM thermal modules were used; parameters of modules have been extracted from the corresponding datasheets provided by Infineon for the switch modules. In Figure 4 are the plots of variations of losses for the switch modules in the inverter-leg topologies with respect to the system modulation index, m. In summary, the inverter-leg in [17] has the highest loss dissipations. The proposed inverter-leg ranks second with about 80% of the highest dissipated total losses in the inverter-leg in [17]. The 5L inverter-leg in [16] incurs the least total losses with about 62% of the highest dissipated losses in its counterpart in [17].

5 | SIMULATION AND EXPERIMENTAL RESULTS

Simulation and experimental studies were carried out on the proposed 3-phase, 5-level active nested neutral point-clamped inverter power circuit in Figure 2. In both studies, the selection criteria for balancing the flying-capacitor voltages (in Table 3) and the presented control steps in Figure 3 were used in the inverter control. Scaled-down system parameters were used in both the simulation and laboratory investigations. Resulting simulated output waveforms of the proposed 5L ANNPC inverter are experimentally validated with a laboratory prototype.

5.1 | Simulation results

Simulation model of the 3-phase power circuit of Figure 2 was developed in PLECS and MATLAB simulation environments. Commensurate logic circuit models were also created using the outlined control scheme in Section 3. The dc-link voltage (V_{dc}) value is 200 V and the three flying-capacitor banks' capacitance is 470 μF. An RL load (R and L are 20 Ω and 20 mH, respectively) is connected in each phase of the inverter, whose modulation index is 0.95; at carrier frequency of 3.3 kHz.

The simulated inverter-leg and line voltages are shown in Figures 5a and 5b, respectively. Therein, the line voltages have 7 voltage steps. Correspondingly, the simulated inverter line current waveforms are displayed in Figure 5c. Waveforms of the blocking voltages across the power switches in phase 'a' are shown in Figure 6. Amongst the eight switches, only switch S_{3a} has voltage stress of 100 V, ($V_{dc}/2$); others have voltage stress of 50 V, ($V_{dc}/4$), each. For the indicated input voltage value, profiles of the flying-capacitor voltage waveforms in phase 'a', along with the inverter-leg voltage, are displayed in Figure 6b; where the deployed control scheme provided good balancing of the capacitor voltages in all the phases. The capacitor voltages' balancing scheme in Table 3 was deactivated at 0.266 s and activated again at 0.286 s. Resulting profiles of the flying-capacitor voltages are shown in Figure 7; wherein good dynamic control operation was obtained.

5.2 | Experimental results

Experimental stand for a scaled-down prototype of the 5L NNPC inverter is shown in Figure 8a; its specifications are given in Table 5. Modulation index value was set to 0.95.

The waveforms of inverter-leg from the 5L NNPC inverter prototype are displayed in Figure 8b. The corresponding line voltages and load current waveforms are shown in Figure 9. In Figure 10a, the displayed blocking-voltage waveforms of switches in phase 'a' agree with the 5L NNPC inverter-leg concept in Figure 1c. The nested capacitor voltage waveforms, together with the inverter-leg voltage, are shown in Figure 10b for phase 'a'.

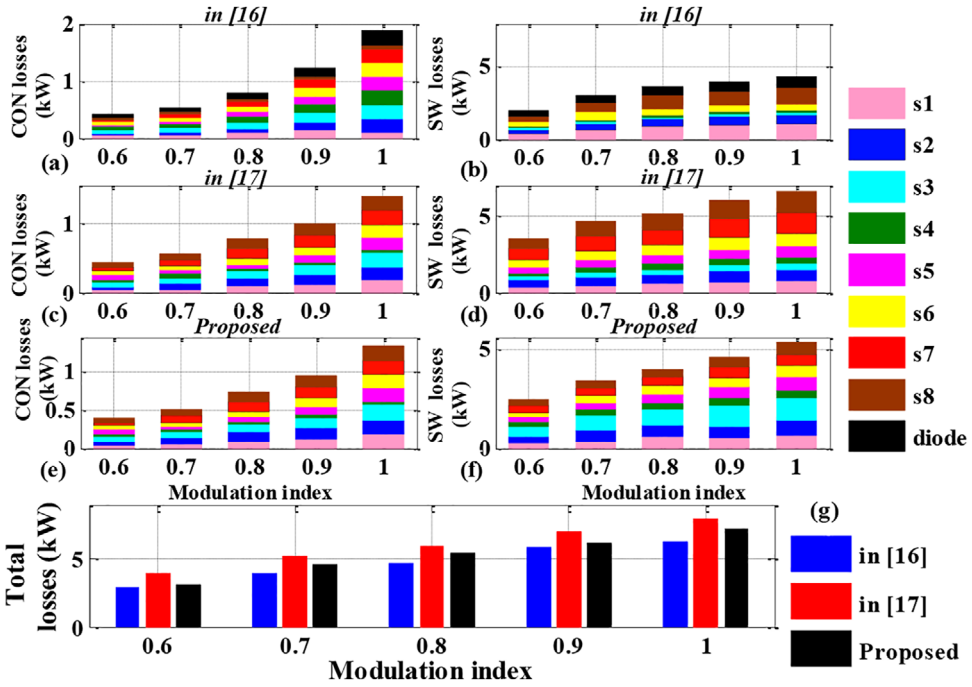

FIGURE 4 Conduction (CON), switching (SW), and total losses of the 5L inverter-legs.

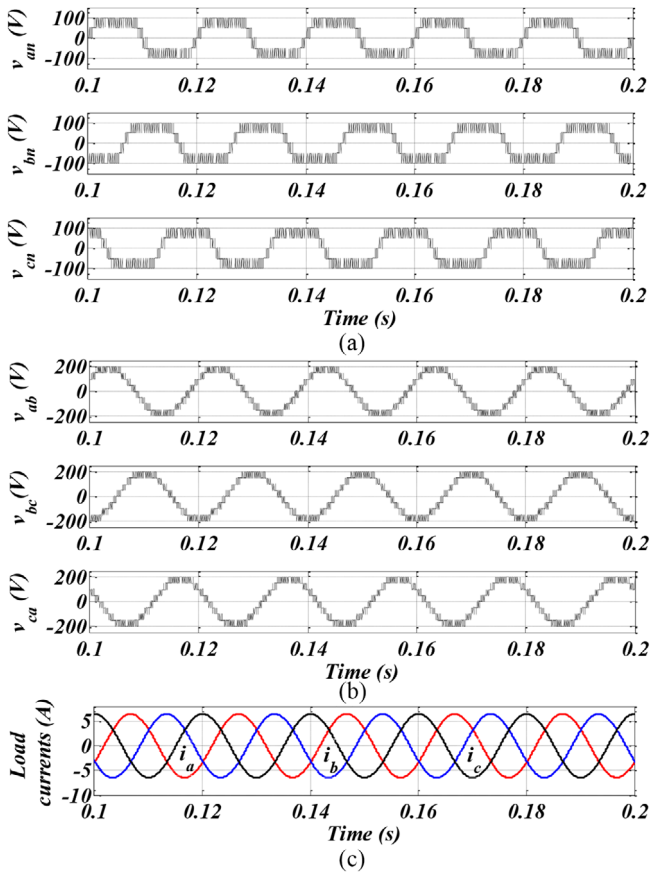

FIGURE 5 Simulated inverter voltage and current waveforms. (a) Inverter-leg voltages; (b) Line voltages; (c) current waveforms.

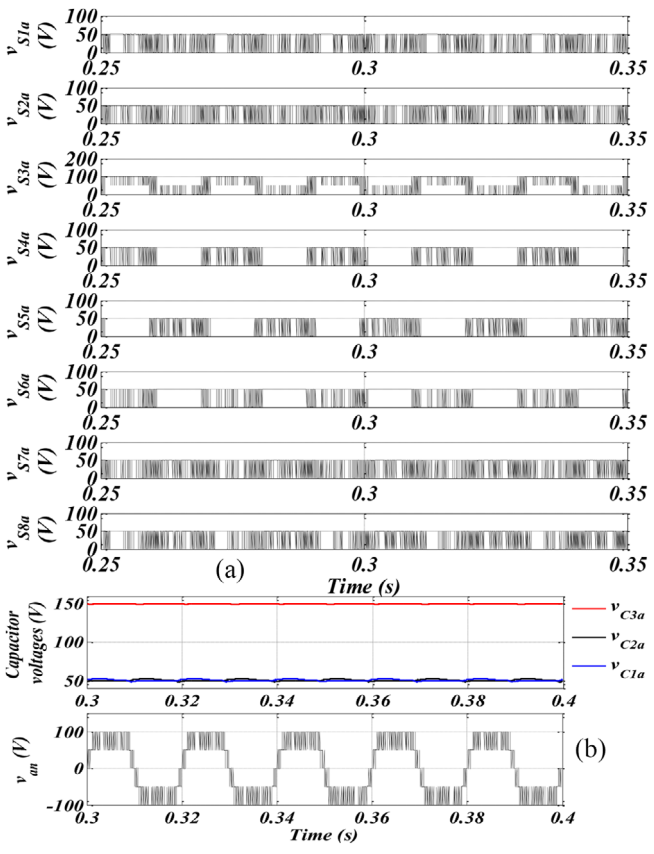

FIGURE 6 Simulated voltage waveforms in phase 'a'. (a) Blocking voltages of all the 8 power switches. (b) Profiles of the flying-capacitor voltages.

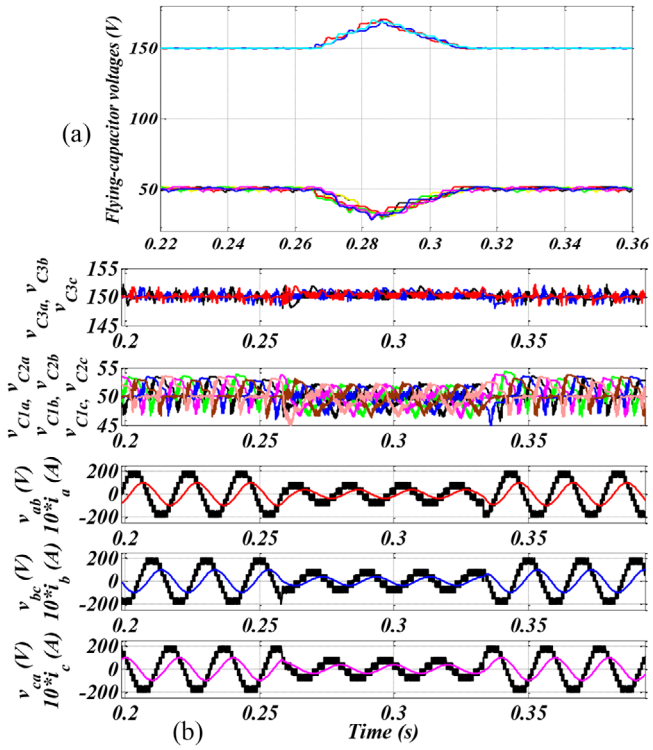

FIGURE 7 (a) Simulated deactivation and activation of the capacitor voltages' balancing scheme. (b) Flying-capacitor, line voltage and current waveforms for step changes in the modulation index: 0.95 to 0.7 and back to 0.95.

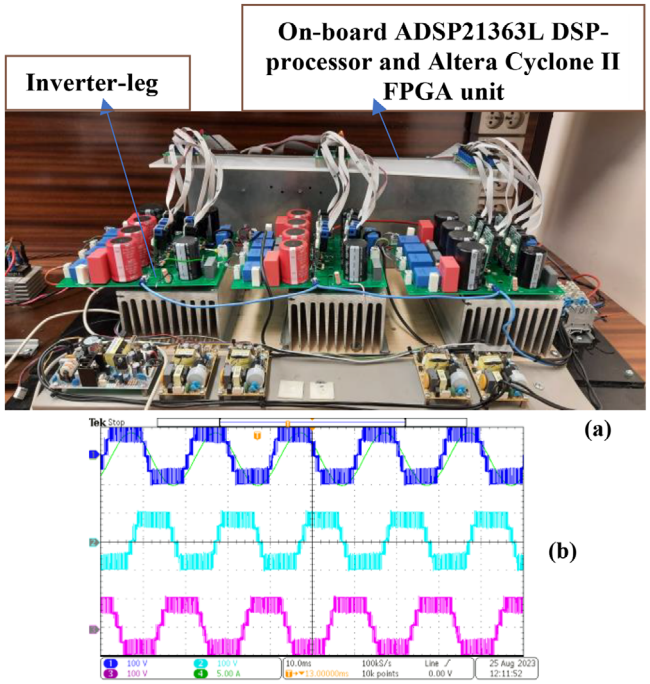

FIGURE 8 Prototype setup and experimental results from the proposed inverter. (a) prototype; (b) Inverter-leg voltages.

TABLE 5 Prototype specification.

Component	Specification
Power switches	AIKW50N60C
Fund. frequency	50 Hz
Carrier frequency	5 kHz
C_1, C_2	470 μF, 600 V
C_3	330 μF, 600 V
Switching frequencyCarrier frequency	3.3 kHz
RL load	20 Ω, 20 mH
Dc-link voltage	200 V

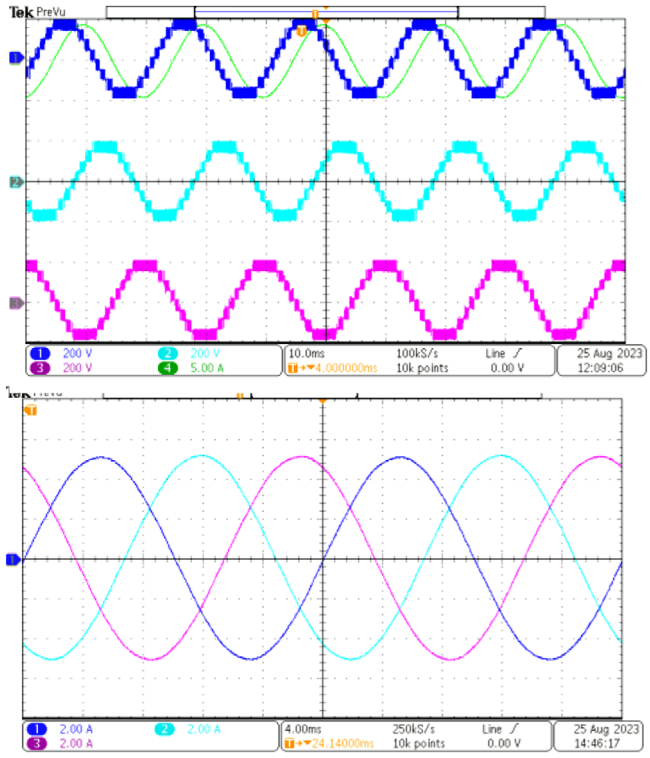

FIGURE 9 Experimental line voltage and current waveforms.

Evidently, these voltage waveforms validate the effectiveness of the deployed modulation scheme in Figure 3. The line voltage frequency spectrum in Figure 10c contains sideband harmonics around the inverter switching frequency of 3.3 kHz.

Deactivation and activation of the capacitors' balancing scheme was experimentally typified in Figure 11a; capacitor voltage profiles for v_{C1a}, v_{C2a}, v_{C3a}, and v_{C3b} were shown. The inverter responded to a dynamic change of modulation index value from 0.95 to 0.7 and back to 0.95 again. In Figure 11b, the number of levels in the output line voltage waveform changes from 9 to 5 and back again to 9. The corresponding load current show decrease and increase in its amplitude values,

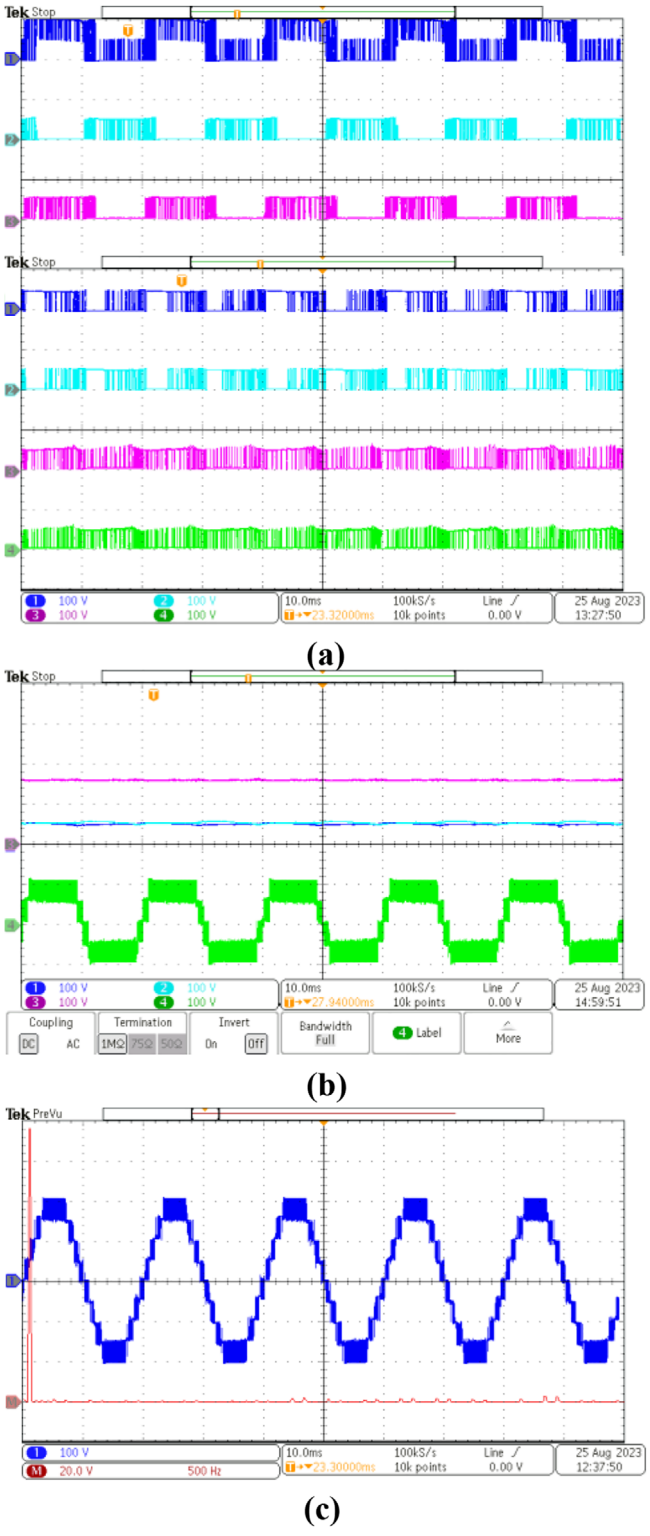

FIGURE 10 Experimental voltage waveforms in phase '*a*'. (a) Blocking voltages of all the 8 power switches. (b) Profiles of the flying-capacitor voltages. (c) FFT spectrum of line voltage v_{ab} waveform.

respectively; but maintained its sinusoidal waveform as shown. Also, the flying-capacitors' voltages were effectively balanced during these dynamic operations, as shown therein.

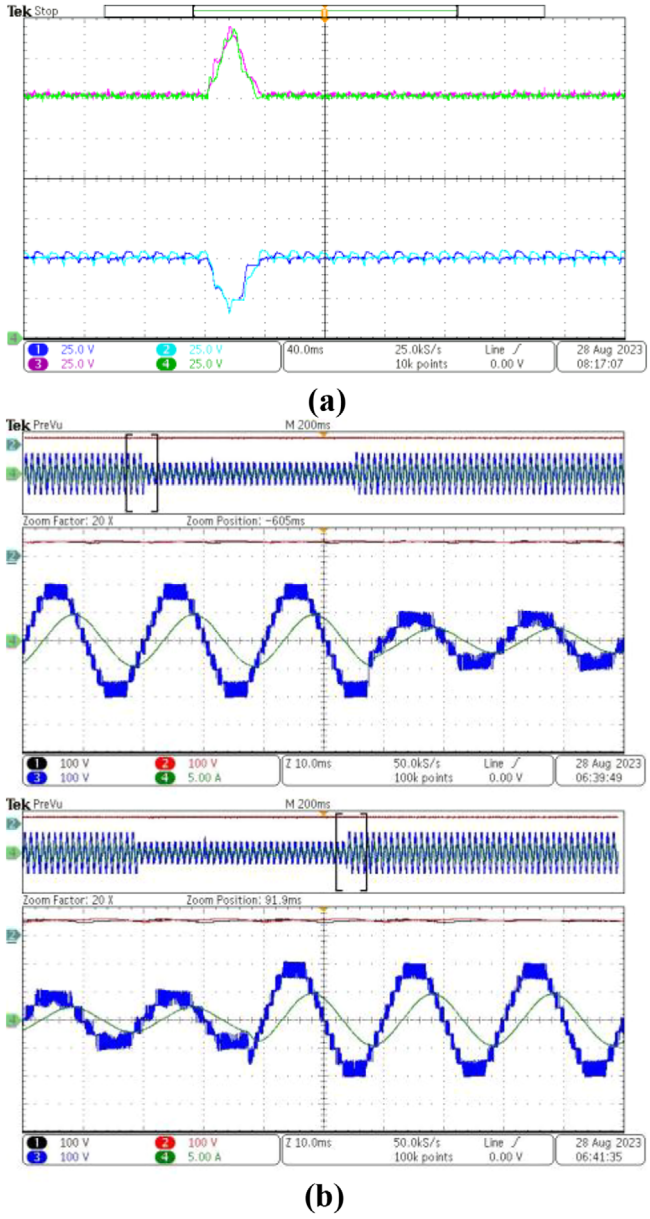

FIGURE 11 (a) Experimental deactivation and activation of the capacitor voltages' balancing scheme. (b) Measured experimental dynamic operational flying-capacitor, line voltage and current waveforms for step changes in the modulation index: 0.95 to 0.7 and back to 0.95.

6 | CONCLUSION

Presented in this paper is a five-level nested neutral-point clamped, 5L NNPC, inverter. Its topological features, operational principle and control scheme have been explained. The innate reduced blocking-voltage on the power switches of this inverter has cost and loss implications. For 6 kV input DC-link voltage and 2 MVA output power rating, it has been shown through cost estimations that the 5L NNPC inverter-leg has the least cost involvement when compared to the five-level inverter-legs proposed in [16] and [17]. Moreover, the same topological feature gave 5L NNPC inverter-leg superior lost performance over its counterpart in [17]. The performance of the proposed

5L NNPC inverter has been presented through simulations and scaled-down experiments on a prototype unit; results have been adequately presented. From the validated performance of the inverter, the prospective future work/application of this inverter will be in the area of high-power, dual-inverter drive system.

AUTHOR CONTRIBUTIONS

Desmond O. Obe: Conceptualization; formal analysis; investigation; methodology; software; writing; funding acquisition. **Chinedu T. Obe**: Formal analysis; investigation. **Charles I. Odeh**: Conceptualization; formal analysis; investigation; methodology; software; writing—review & editing. **Emeka S. Obe**: Formal analysis; project administration; supervision.

CONFLICT OF INTEREST STATEMENT

The authors declare no conflicts of interest.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are openly available in IEEE Xplore library at https://ieeexplore.ieee.org/Xplore/home.jsp

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