

A Fourier Series-Based Steady-State Thermal Resistance Model for Power Module

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Abstract—The finite-element method (FEM) is conventionally employed to evaluate the thermal performance of power modules (TPPM), but it demands substantial computational resources and time. This study introduces a novel approach for TPPM assessment through a Fourier series-based steady-state thermal resistance model (FSS-TRM), which offers enhanced computational efficiency and accuracy. The FSS-TRM integrates conduction and spreading resistance via a mathematical–physical method, explicitly focusing on redefining conduction resistance to optimize computational efficiency. The accuracy of the FSS-TRM is ensured by solving the heat conduction differential equation to obtain spreading resistance. To assess the reliability of the FSS-TRM, the model is tested across varying direct bonded copper (DBC) configurations and chip sizes. Experimental results reveal that the maximum error of the FSS-TRM compared with the conventional COMSOL approach is below 4%. In addition, the FSS-TRM’s capability to predict TPPM is verified through testing a representative power module in a 34-mm package, demonstrating an error of only 0.9% compared with both COMSOL and experimental results. Notably, the computational efficiency of the FSS-TRM is significantly improved, excelling COMSOL by five orders of magnitude. Therefore, the proposed FSS-TRM provides an accurate and efficient alternative to FEM for TPPM estimation.

Index Terms—Fourier series, power module, steady-state thermal resistance, thermal performance, thermal resistance model.

I. INTRODUCTION

POWER modules, the critical component of modern electronic devices, have been widely used across industries, such as industrial control [1], transportation [2], and renewable energy [3]. However, the drive to increase the operating frequency and switching speed of wide-bandgap semiconductors, coupled with the need to reduce chip size, has significantly increased heat flux per unit area of power chips [4]. This phenomenon poses a significant challenge to thermal management in high-power applications, where multiple power chips are interconnected in parallel to increase current capacity, leading to further heat generation within the power module [5], [6], [7]. Consequently, thermal management and design have assumed pivotal roles in power module development and have become critical in further advancements in the field.

Thermal resistance is an essential parameter for estimating the thermal performance of power modules (TPPM) [8], [9], [10]. In thermal design, the finite-element method (FEM) and the traditional Cauer thermal network model are widely recognized as the primary methods for calculating the thermal resistance in power modules [11], [12], [13]. However, FEM exhibits resource-intensive and time-consuming attributes, thereby elongating the duration needed for optimizing thermal design [14]. Similarly, the traditional Cauer thermal network model heavily relies on heat transfer area, which can pose challenges in accurate determination, resulting in thermal resistance calculation errors [15], [16]. Therefore, there is an urgent need for an efficient and accurate method to evaluate the thermal resistance of power modules.

In recent years, the heat spreading angle has emerged as a vital parameter for describing the heterogeneous characteristics of physical material layers and improving the accuracy of heat transfer area calculations [17]. Previous studies have suggested that a fixed heat spreading angle of 45° can result in a 30% improvement in thermal resistance prediction compared with the traditional Cauer thermal network model [18]. However, Schweitzer and Chen [19] and Vermeersch and De Mey [20] have pointed out that heat spreading angles may not be identical in all heterogeneous layers. In [21], the heat spreading angle was determined as the inverse tangent of the ratio of the thermal conductivity of the layer to that of the next layer, resulting in a further

Manuscript received 12 December 2023; revised 8 March 2024 and 5 April 2024; accepted 2 May 2024. Date of publication 8 May 2024; date of current version 2 August 2024. This work was supported in part by the National Natural Science Foundation of China under Grant 62174134; in part by the Shaanxi Innovation Capability Support Project under Grant 2021TD-25; in part by the Xi’an Key Industrial Chain Key Core Technology Research under Grant 23LLRH0044; in part by the Science and Technology–Natural Science Foundation of Shaanxi Province under Grant 2022JQ-360; in part by the Spanish Administration Projects under Grant PID2021-125628OB-C22 and Grant TED2021-130610B-C21 (MCIN/AEI/10.13039/501100011033/FEDER, UE, and “NextGenerationEU/PRTR”); and in part by BRONTE, cofinanced by the Junta de Comunidades de Castilla La Mancha and the European Union (EU) through the European Research and Development Funds (ERDF), under Grant SBPLY/21/180501/000147. Recommended for publication by Associate Editor Tsuyoshi Funaki. (*Corresponding author: Yuan Yang.*)

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Color versions of one or more figures in this article are available at <https://doi.org/10.1109/JESTPE.2024.3398440>.

Digital Object Identifier 10.1109/JESTPE.2024.3398440

20% increase in the accuracy of thermal resistance calculation compared with the previous study [18]. This method enables more precise estimation of the heat transfer area and quick computation of thermal resistance. However, despite its advantages, its accuracy still requires improvement compared with the FEM.

For decades, the mathematical–physical method has served as a well-established approach in microelectronics, facilitating the exploration of analytical solutions for thermal resistance [22]. This versatile method derives a general solution for thermal resistance based on physical properties, such as package structure and material properties. Notably, Kennedy [23] exemplified this by obtaining an analytic solution for thermal resistance in a cylindrical baseplate with a circular heat source and an isothermal bottom, a model widely adopted in industrial package design. Similarly, Muzychka et al. [24] formulated a mathematical model for the thermal resistance of a double-layer rectangular baseplate. Furthermore, many researchers have also employed this method to characterize TPPM. For example, Gerstenmaier and Wachutka [25] used the eigenvalue method, Gerstenmaier et al. [26] employed Green’s function method, and Choudhury and Rogers [27] used the Fourier series method to obtain 3-D temperature distribution expression for power modules. These approaches can obtain high-precision chips junction temperature distribution within minutes, representing a significant breakthrough compared with FEM. However, using these methods to calculate the thermal resistance is time-consuming. According to the definition of thermal resistance, it is necessary to calculate not only the junction temperature but also the case temperature of the power module. Second, the functions of junction and case temperatures are expressions with respect to the number of orders, and the coefficients of these functions are also functions with respect to the number of orders.

In order to facilitate a faster and more accurate evaluation of TPPM, we propose a novel approach called Fourier series-based steady-state thermal resistance model (FSS-TRM). This method allows for efficient thermal performance evaluation within a minute without the need to calculate the temperature field of the entire power module. In addition, FSS-TRM can quickly produce package size-thermal resistance charts by scanning package size parameters, which can be used in power module thermal optimization design. The contributions of this work are summarized as follows.

- 1) We introduce the power module thermal resistance model (FSS-TRM), which is founded on a Fourier series-based 3-D temperature distribution model. In contrast to conventional methods for calculating thermal resistance, our model eliminates the need to calculate the case temperatures to calculate thermal resistance.
- 2) We employ conduction and spreading resistance to construct the proposed FSS-TRM. Specifically, we redefine the expression for conduction resistance to streamline the FSS-TRM and improve computational efficiency. We then apply the separation of variables and Fourier series methods to derive expressions for spreading resistance, resulting in more accurate evaluations.

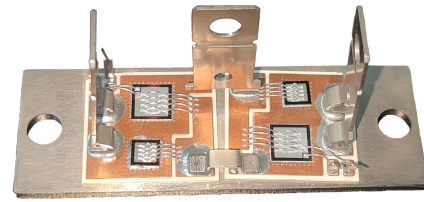


Fig. 1. Commercial 34-mm packaged power module manufactured by CRRC.

- 3) The FSS-TRM, a mathematical–physical-based approach to enable rapid and precise evaluation of the TPPM. This approach has the potential to substantially shorten the power module design timeline.

The article is structured as follows. Section II will introduce the challenges in calculating thermal resistance using the 3-D temperature distribution method and the necessity of constructing the FSS-TRM. In Section III, the FSS-TRM will be constructed based on the mathematical–physical method from the perspective of the spreading and conduction resistance. In Section IV, the reliability of FSS-TRM will be verified by convergence and general applicability comparison with the FEM method (COMSOL) under different direct bonded copper (DBC) and die sizes. Moreover, the effectiveness and efficiency of FSS-TRM will be tested using the commercial 34-mm package modules and making a comparison with experimental and COMSOL results.

II. CONSTRUCTION OF THE TEMPERATURE DISTRIBUTION

Silicon (Si)-insulated gate bipolar transistor (IGBT) power electronic modules are categorized into two types of packaging: soldered and press pack. Among them, soldered packaging power modules have a more extensive range of applications due to their low cost and high performance. As an example, consider the typical 34-mm packaged IGBT power modules, characterized by a multilayer composite structure encompassing a power chip, chip solder, DBC, DBC solder, and baseplate, as illustrated in Fig. 1. The DBC consists of three layers, including a copper layer, ceramic layer, and another copper layer. In line with [27], this study adopts a seven-layer rectangular structure model to effectively represent the intricate module structure, as depicted in Fig. 2.

It is important to highlight that FSS-TRM is developed based on the Fourier series-based 3-D temperature distribution, and introducing the construction of the 3-D temperature distribution is crucial for a comprehensive understanding of FSS-TRM. The model uses a heat conduction differential equation with appropriate boundary conditions to describe TPPM. This section provides a detailed explanation of the development of the Fourier series-based 3-D temperature distribution model, focusing on the construction of the model from the perspective of the governing equation and boundary conditions.

A. Governing Equation

In describing TPPM, 3-D unsteady heat conduction equation in Cartesian coordinates according to Fourier’s law of heat conduction was introduced, given as follows:

$$\rho c \frac{\partial T}{\partial t} = \frac{\partial}{\partial x} \left(\lambda \frac{\partial T}{\partial x} \right) + \frac{\partial}{\partial y} \left(\lambda \frac{\partial T}{\partial y} \right) + \frac{\partial}{\partial z} \left(\lambda \frac{\partial T}{\partial z} \right) + \dot{\phi} \quad (1)$$

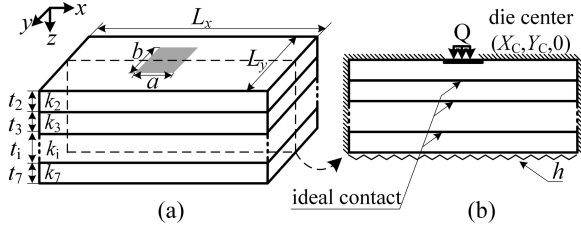


Fig. 2. FSS-TRM model. (a) Coordinate system for power module. (b) Compound channel with rectangular heat source.

where ρ is the density, c is the specific heat, T is the temperature, t is the time, and ϕ is the amount of heat generated by a unit volume in a unit time.

However, this is a general equation with which all thermal conductivity conditions can be satisfied. In this article, we assume that thermal resistance and heat transfer coefficient do not change with time. Thus, (1) can be simplified to the following Laplace's equation:

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} = 0. \quad (2)$$

B. Boundary Conditions

The heat conduction problem essentially involves solving the heat conduction differential equation, i.e., (2). However, to obtain the temperature distribution of the power module, it is necessary to provide certain physical descriptions that characterize the heat transfer properties of the power module. These physical descriptions, known as boundary conditions, are as follows:

- 1) Each layer of the structure is rectangular and has the same lateral dimensions. However, the thickness of each layer may differ.
- 2) The open surfaces of the structure are adiabatic. In other words, the heat exchange is only by conduction, so the heat losses due to radiation and convection are zero inside the structure.
- 3) The dies are the only heat source, and heat is generated at the top surface of the chip. The thickness of the heat source is assumed to be zero.
- 4) The contact of adjacent layers in the structure is in ideal contact. The thermal contact resistance is zero, with the temperature and the heat flux being equal through the interface.
- 5) The material exhibits isotropic properties, and its thermal properties remain constant regardless of temperature.

Based on these conditions, the 3-D rectangular model depicted in Fig. 2 is constructed to simplify the physical model of the power module. A Cartesian coordinate system is used to describe the basic scale of the module, where the length of the power chip is represented by a and the width by b . In addition, the length and width of each layer, except for the chip, are defined by L_x and L_y , respectively, while the thickness of the i th layer is denoted by t_i . To locate the die on the substrate, the center of the chip is given by $(X_C, Y_C, 0)$.

In addition to the basic physical dimensions, various variables must be considered to define the heat properties.

Specifically, the thermal conductivity of the i th layer is defined as k_i , while the heat exchange at the bottom of the module is through convection and has a convection coefficient of h . The ambient temperature is represented as T_f , and the heat generated by the chip is Q . In addition, the area and temperature of the chip are A_s and T_j , respectively. Therefore, the above description can be represented mathematically as follows:

$$\frac{\partial T}{\partial x} \Big|_{x=0, L_x} = \frac{\partial T}{\partial y} \Big|_{y=0, L_y} = 0. \quad (3)$$

The equation describes that the open surfaces of the structure are adiabatic, i.e., the heat loss is zero at the four surfaces $x = 0$, $x = L_x$, $y = 0$, and $y = L_y$. Following the first-class boundary condition of heat transfer law, (3) can be obtained. This boundary condition is called the Dirichlet Condition in mathematical physics theory

$$-k_1 \frac{\partial T_1}{\partial z} \Big|_{z=0, x=X_C \pm a/2, y=Y_C \pm b/2} = \frac{Q}{A_s} \quad (4)$$

$$k_i \frac{\partial T_i}{\partial z} \Big|_{z=z_i} = k_{i+1} \frac{\partial T_{i+1}}{\partial z} \Big|_{z=z_i} \quad (5)$$

$$T_i(x, y, z_i) = T_{i+1}(x, y, z_i). \quad (6)$$

Equations (5) and (6) describe the relationship between the heat flow density and temperature continuum at the interface of two materials, respectively. In simpler terms, the layers in contact have good interfacial contact, i.e., equal heat flow densities and temperatures at the interface. This boundary condition is called the interfacial continuum condition in thermal conduction theory

$$z_i = \sum_{j=1}^i t_j, \quad i = 1 \sim 7 \quad (7)$$

$$k_7 \frac{\partial T_7}{\partial z} \Big|_{z=z_7} = -h [T_7|_{z=z_7} - T_f]. \quad (8)$$

The equation illustrates the cooling of the model's bottom surface. Applying the third-class boundary condition of heat transfer, (8) is derived. This condition is known as the Robin condition in mathematical physics theory

$$\frac{\partial T_1}{\partial z} \Big|_{z=0, x \neq X_C \pm a/2, y \neq Y_C \pm b/2} = 0. \quad (9)$$

Equations (4) and (9) depict energy injection at the chip location, with no energy injection outside the chip, making the chip the only heat source. Consequently, obtaining this expression is straightforward based on the second-class boundary conditions of heat transfer. This boundary condition is known as the Neumann condition in mathematical physics theory.

C. 3-D Temperature Distribution Calculation

In this section, the process of the temperature general solution will be elucidated, and the challenges will be introduced in calculating thermal resistance using the 3-D temperature

distribution method and the necessity of constructing the FSS-TRM. First, the 3-D temperature distribution is solved as follows.

The excess temperature is introduced to simplify the solution process, allowing for the transformation of (8) into a homogeneous boundary condition

$$\theta_i = T_i - T_f \quad (10)$$

where T_i is the temperature of the i th layer and T_f is the ambient temperature. Thus, (2) can be further written as follows:

$$\frac{\partial^2 \theta_i}{\partial x^2} + \frac{\partial^2 \theta_i}{\partial y^2} + \frac{\partial^2 \theta_i}{\partial z^2} = 0. \quad (11)$$

To address the Laplace equation, the separating variable method is used. Therefore, the separated variable form of (11) can be expressed as follows:

$$\theta_i(x, y, z) = X_i(x)Y_i(y)Z_i(z). \quad (12)$$

According to the solution of the second-order constant coefficient homogeneous linear differential equation, the general temperature expression can be obtained, which satisfies (3)

$$\begin{aligned} \theta_i(x, y, z) = & A_{i,0} + B_{i,0}z_i \\ & + \sum_{m=1}^{\infty} \cos(\alpha_m x) [A_{i,m} \cosh(\alpha_m z_i) + B_{i,m} \sinh(\alpha_m z_i)] \\ & + \sum_{n=1}^{\infty} \cos(\beta_n y) [A_{i,n} \cosh(\beta_n z_i) + B_{i,n} \sinh(\beta_n z_i)] \\ & + \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \cos(\alpha_m x) \cos(\beta_n y) [A_{i,mn} \cosh(\gamma_{mn} z_i) \\ & \quad + B_{i,mn} \sinh(\gamma_{mn} z_i)] \end{aligned} \quad (13)$$

where $\alpha_m = m\pi/L_x$, $\beta_n = n\pi/L_y$, and $\gamma_{mn} = ((\alpha_m^2 + \beta_n^2))^{1/2}$.

According (13), the junction and case temperature of the power module can be expressed as follows:

$$\begin{aligned} T_j &= T_1 = \theta_1 + T_f \\ T_c &= T_7 = \theta_7 + T_f \end{aligned} \quad (14)$$

where T_j is the temperature of the chip junction and T_c is the power module case temperature.

By definition the junction–case thermal resistance can be expressed as follows:

$$R = (T_j - T_c)/Q. \quad (15)$$

Based on (14) and (15), employing the thermal resistance approach to evaluate the TPPM requires calculating not only θ_1 but also θ_7 . In contrast, only θ_1 is needed to assess the TPPM using the junction temperature of the chip. This indicates an increase in computational time when using the thermal resistance method for TPPM assessment. In addition, the challenge posed by a Fourier series-based model lies in solving the Fourier coefficients, such as $A_{i,0}$, $B_{i,0}$, $A_{i,m}$, $B_{i,m}$, $A_{i,n}$, $B_{i,n}$, $A_{i,mn}$, and $B_{i,mn}$. Acquiring the $A_{i,0}$ coefficients proves to be a difficult task, as indicated in [27], which provides

a detailed procedure for solving both A and B coefficients. In response, Choudhury and Rogers [27] further simplified the model to two layers, albeit introducing inherent errors, to obtain the $A_{i,0}$ coefficients. In response to these challenges, this article proposes an FSS-TRM model, which will be elaborated upon in Section III.

III. CONSTRUCTION OF THE FSS-TRM

In Section II-C, employing the Fourier series-based thermal resistance for assessing TPPM presents two notable challenges: the difficulty in solving $A_{i,0}$ and the time-consuming cause of solving θ_1 and θ_7 simultaneously. This section introduces the construction of the FSS-TRM model to solve these problems. The selection of appropriate assumptions is crucial to obtain the FSS-TRM model with simplified equations while preserving the physical integrity of the problem. Within the FSS-TRM, only θ_1 needs to be solved. Hence, the required computation time for evaluating the TPPM was reduced.

Furthermore, we discovered that the thermal resistance of the power module could be composed of conduction and spreading resistance through the analysis of the 3-D temperature distribution expression, in which the $A_{i,0}$ coefficient plays a significant role in the conduction resistance. Building on this analysis, we redefine the conduction resistance, eliminating the need to solve for the $A_{i,0}$ coefficient. Sections III-A and III-B describe each of these areas in detail.

A. Addressing the First Challenge

According to (15), accurately characterizing thermal resistance requires precise values for both parameters, θ_1 and θ_7 . However, in thermal resistance physical descriptions, the emphasis is primarily on temperature gradients, prioritizing the difference between θ_1 and θ_7 over their specific values, despite the equal importance of obtaining accurate values for both. Guided by this, we modify the thermal boundary conditions by increasing the convection coefficient. Consequently, θ_1 and θ_7 concurrently decrease while maintaining a constant difference. When the convection coefficient is high enough, the baseplate temperature of the power module equals the ambient temperature, indicating that θ_7 is a constant. In such instances, only θ_1 needs to be solved. Therefore, the above description can be represented mathematically as follows:

$$\begin{aligned} R &= (T_j - T_c)/Q = (T_1 - T_7)/Q \\ &= ((\theta_1 + T_f) - (\theta_7 + T_f))/Q. \end{aligned} \quad (16)$$

If convection coefficient h is large enough, $T_c \approx T_f$. Thus, (16) can be simplified as follows:

$$R = \theta_1/Q. \quad (17)$$

It is essential to mention that this article uses (15) and (17) to experimentally test the power module thermal resistance and construct the FSS-TRM, respectively. Equations (15) and (17) primarily arise from variations in heat dissipation conditions, i.e., the difference in convection coefficients. However, the thermal resistance values of the power module derived using these two equations are identical.

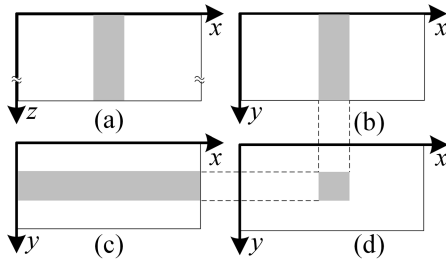


Fig. 3. General solution of temperature. (a) Linear solution. (b) Single summation in the y -direction. (c) Single summation in the x -direction. (d) Double summation solution.

B. Addressing the Second Challenge

Although using (17) to evaluate the TPPM improves computational efficiency, it faces a challenge similar to that mentioned in [27], which involves solving for the $A_{i,0}$ coefficient. To address this problem, (13) was further analyzed.

First, the components of the general expression for the temperature consist of four parts, which include a linear solution and three superposition solutions. The linear solution describes heat transfer in the z -direction, representing 1-D heat conduction, as depicted in Fig. 3(a). The superposition solutions describe heat transfer in the x - and y -directions while incorporating the z_i variables. Unlike the z_i variables in the linear solution, the z_i variables in the superposition solutions describe heat transfer in the x - and y -directions at a distance z_i from the heat source. Therefore, the superposition solutions can be understood as heat diffusion, with the single summation representing transfer in the x - and y -directions, as shown in Fig. 3(b) and (c), respectively. The double summation describes transfer from the heat source, as shown in Fig. 3(d).

Based on the above analysis, the thermal resistance of the power module consists of two parts: 1-D thermal resistance for heat conduction in the z -direction and spreading thermal resistance for heat conduction in the x - and y -directions. It is essential to note that the thermal resistance of power modules mentioned in this article only includes conduction thermal resistance. This is because within power modules, conduction thermal resistance typically prevails, while the influence of air and thermal radiation can be neglected. It can be expressed in the following form:

$$R = \theta_1/Q = \frac{\theta_{1_line}}{Q} + \frac{\theta_{1_superposition}}{Q} = R_{1D} + R_s \quad (18)$$

where θ_{1_line} is the linear solution of θ_1 , $\theta_{1_superposition}$ is the superposition solution of θ_1 , R_{1D} is the conduction resistance, and R_s is the spreading resistance. Then, the solution processes for R_{1D} and R_s will be explained in detail, where the second challenge is addressed in R_{1D} .

1) *Conduction Resistance Calculation*: To address the challenge of solving the $A_{i,0}$ coefficients and improve the computational efficiency by reducing the complexity of the model, it can be concluded from the above analysis that the solution involving $A_{i,0}$ coefficients represents the heat conduction in the z -direction in a 1-D space. Based on the

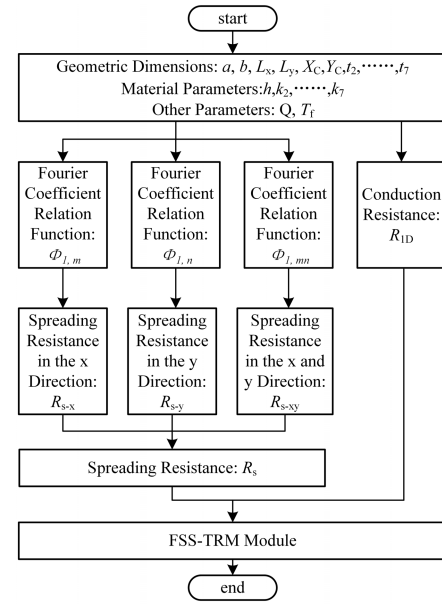


Fig. 4. Computational workflow of the FSS-TRM in MATLAB.

above analysis and experimental results, R_{1D} can be defined as follows:

$$R_{1D} = \sum_{i=1}^7 t_i / (k_i A) \quad (19)$$

where $A = L_x \cdot L_y$.

2) *Spreading Resistance Calculation*: This section illustrates the computation of spreading resistance. Since the solving process for superposition solutions is similar according to (13), this section focuses on presenting the solution process for the x -direction. Referring to (18), the spreading resistance can be expressed as follows:

$$R_s = \bar{\theta}_{1_superposition} / Q \quad (20)$$

where $\bar{\theta}_{1_superposition}$ is the mean temperature of $\theta_{1_superposition}$. It can be written as follows:

$$\bar{\theta}_{1_superposition} = \frac{1}{ab} \int_{X_c - \frac{a}{2}}^{X_c + \frac{a}{2}} \int_{Y_c - \frac{b}{2}}^{Y_c + \frac{b}{2}} \theta_1(x, y, 0) dx dy. \quad (21)$$

Thus, the $\bar{\theta}_{1_superposition}$ in the x -direction can be written as follows:

$$\begin{aligned} \bar{\theta}_{1_superposition-x} &= \sum_{m=1}^{\infty} \frac{1}{ab} \int_{X_c - \frac{a}{2}}^{X_c + \frac{a}{2}} \int_{Y_c - \frac{b}{2}}^{Y_c + \frac{b}{2}} A_{1,m} \cos(\alpha_m x) dx dy \\ &= \sum_{m=1}^{\infty} \frac{8Q \cos^2(\alpha_m X_c) \sin^2(\alpha_m \frac{a}{2})}{a^2 L_x L_y K_1 \alpha_m^3} \cdot \Phi_{1,m} \end{aligned} \quad (22)$$

where $\Phi_{1,m}$ represents the relationship between $A_{1,m}$ and $B_{1,m}$. More derivation details are provided in the Appendix. Hence,

$$R_{s-x} = \sum_{m=1}^{\infty} \frac{8 \cos^2(\alpha_m X_c) \sin^2(\alpha_m \frac{a}{2})}{a^2 L_x L_y K_1 \alpha_m^3} \cdot \Phi_{1,m}. \quad (23)$$

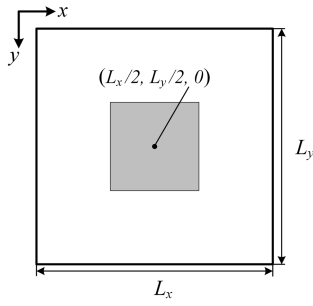


Fig. 5. Top view of the FSS-TRM.

Thus, the spreading resistance can be obtained

$$\begin{aligned}
 R_s = & \sum_{m=1}^{\infty} \frac{8\cos^2(\alpha_m X_c)\sin^2(\alpha_m \frac{a}{2})}{a^2 L_x L_y K_1 \alpha_m^3} \cdot \Phi_{1,m} \\
 & + \sum_{n=1}^{\infty} \frac{8\cos^2(\beta_n Y_c)\sin^2(\beta_n \frac{b}{2})}{b^2 L_x L_y K_1 \beta_n^3} \cdot \Phi_{1,n} \\
 & + \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \frac{64\cos^2(\alpha_m X_c)\sin^2(\alpha_m \frac{a}{2})\cos^2(\beta_n Y_c)\sin^2(\beta_n \frac{b}{2})}{a^2 b^2 L_x L_y K_1 \alpha_m^2 \beta_n^2 \gamma_{mn}} \\
 & \cdot \Phi_{1,mn}. \quad (24)
 \end{aligned}$$

The spreading resistance of the power module can be determined using the expression presented above, which indicates how the resistance is related to the system's thermal and geometric parameters. It should be noted that the location of the die on the DBC can affect the resistance.

Based on the above, the FSS-TRM can be derived from (19) and (24) and implemented using MATLAB software. The computational workflow of the FSS-TRM in MATLAB is illustrated in Fig. 4.

IV. EXPERIMENT AND ANALYSIS

A. FSS-TRM Reliability Verification Using FEM

In this section, we conduct convergence testing and investigate errors for various DBC and die sizes using the FSS-TRM presented in Section III. It is worth noting that the errors are all based on COMSOL FEM software, and mesh selection in COMSOL is performed with an extremely finite-element size. In this section, it is crucial to note that, for a clearer validation test of FSS-TRM reliability, we assume that the chip consistently resides at the center of the baseplate, as depicted in Fig. 5. Importantly, this assumption is specific to this section.

1) *Convergence Tests*: To balance accuracy and time cost, the convergence of the FSS-TRM was evaluated for various DBC sizes using the variables m , n , L_x , and L_y . Specifically, the variables are set as follows: $m = n$ and $L_x = L_y$. Furthermore, the die size is constant, $a = b = 4$ mm.

Fig. 6 shows the convergence of the FSS-TRM at different truncation orders (m and n). The error decreases with the number of truncation orders, with a rapid reduction in Fig. 6(a) and (b), and a slower reduction in Fig. 6(c) and (d). Based on the results, the model converges after 30 truncation orders, consistent with previous studies [28]. Fig. 6(c) demonstrates an error of only 0.5%, indicating a junction

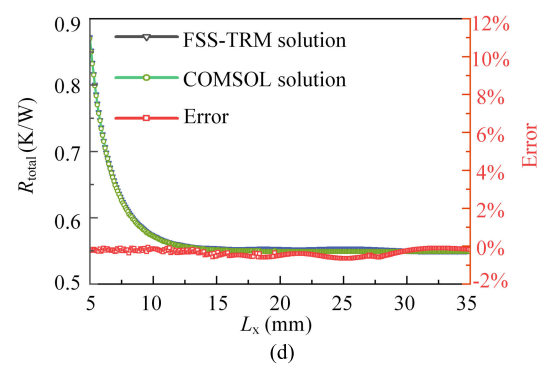
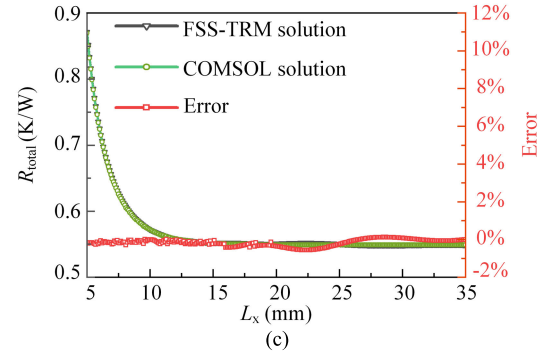
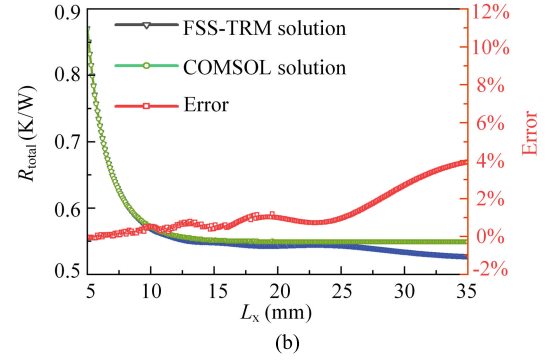
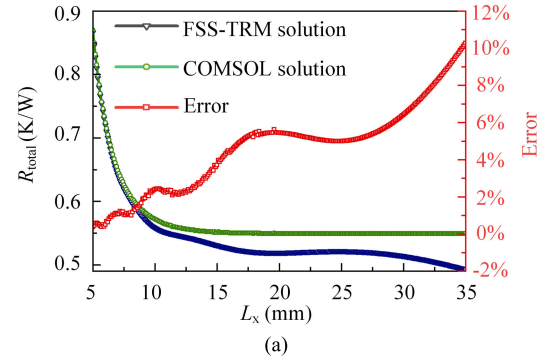


Fig. 6. Convergence tests of the FSS-TRM. (a) FSS-TRM truncation orders 10. (b) FSS-TRM truncation orders 20. (c) FSS-TRM truncation orders 30. (d) FSS-TRM truncation orders 40.

temperature error of less than 1 °C. While the error accuracy improves slightly in Fig. 6(d) by 0.1%, it comes at the cost of a 20% increase in computational time. Therefore, this study selects a truncation order of 30.

In addition, it can be observed from Fig. 6 that the resistance exhibits an exponential decrease for DBC sizes below 20 mm, followed by a stabilization for DBC sizes above 20 mm. This behavior is attributed to thermal spreading. To gain

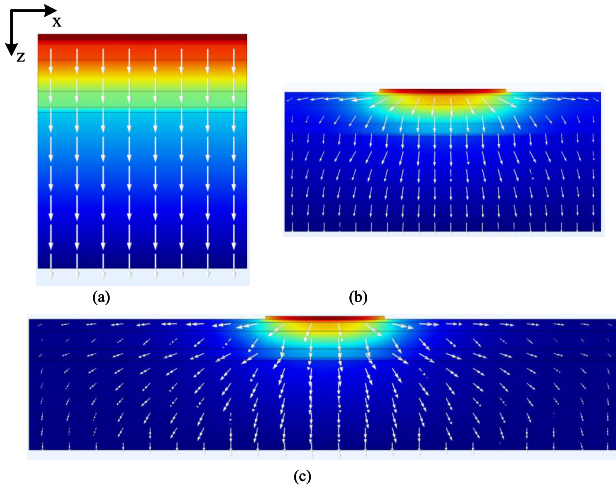


Fig. 7. 3-D heat flux vector distribution results by the COMSOL. (a) $L_x = L_y = a = b = 4$ mm. (b) $L_x = L_y = 10$ and $a = b = 4$ mm. (c) $L_x = L_y = 20$ and $a = b = 4$ mm.

further insights into this phenomenon, the heat flow density distributions and the temperature distribution are computed using COMSOL for the three cases, as depicted in Fig. 7.

Fig. 7 shows the heat flow density vector using white arrows. Specifically, Fig. 7(a) presents the case without thermal spreading, where the direction and size of the white arrows remain unchanged with the z -direction. In contrast, Fig. 7(b) and (c) depicts arrow direction and size variation along the z -direction, indicating the occurrence of thermal spreading. Notably, the arrows in Fig. 7(c) are considerably smaller than those in Fig. 7(b) at the furthest distance from the chip in the x -direction. This observation implies that thermal spreading in Fig. 7(c) has reached its maximum extent, and the arrows can be considered negligible. These findings are consistent with the previous convergence test.

2) *General Applicability Test*: To test the general applicability of the FSS-TRM, different DBC sizes are utilized, similar to the convergence tests, except L_x and L_y are not always equal. The parameters are set as follows: $m = n = 30$, $X_C = L_x/2$, $Y_C = L_y/2$, and $a = b = 4$ mm, and the results are shown in Fig. 8. The black line in Fig. 8 represents the error compared with COMSOL. It is evident that the error is less than 1% when the aspect ratio of DBC is less than 5 (e.g., $L_x = 5$ mm and $L_y \leq 25$ mm), and the error range is between 2% and 4% when the aspect ratio of DBC is greater than 5 (e.g., $L_x = 5$ mm and $L_y \geq 25$ mm). This result is due to the overestimation of the adequate heat spreading area evaluated in the conduction resistance, leading to the underestimation of the thermal resistance. It is worth noting that the aspect ratio of DBC will not exceed 5 in the power module design.

To further investigate the general applicability of the FSS-TRM, experiments were carried out for different chip sizes. Specifically, the variables a and b were varied while keeping $m = n = 30$, $L_x = L_y = 35$ mm, $X_C = L_x/2$, and $Y_C = L_y/2$. The results in Fig. 9 demonstrate the relationship between thermal resistance and chip size. The black line in Fig. 9 represents the error compared with COMSOL. The maximum error in the calculation is less than 2%, which falls within the acceptable limits. Notably, the error is less than 1% when

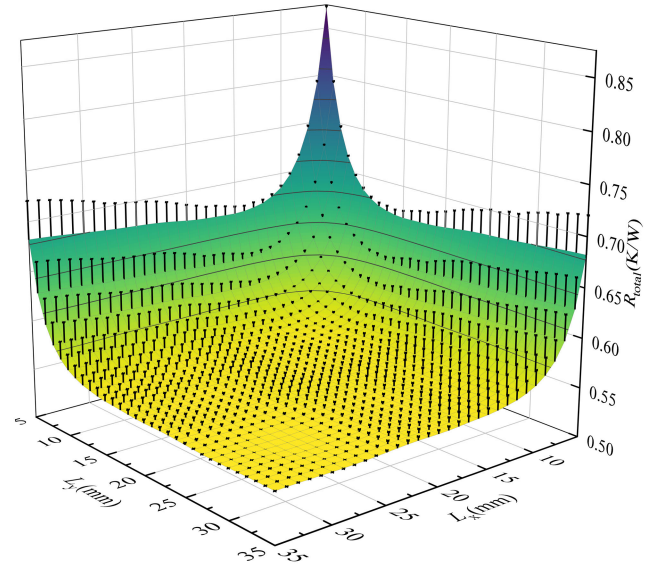


Fig. 8. Effect of different DBC sizes.

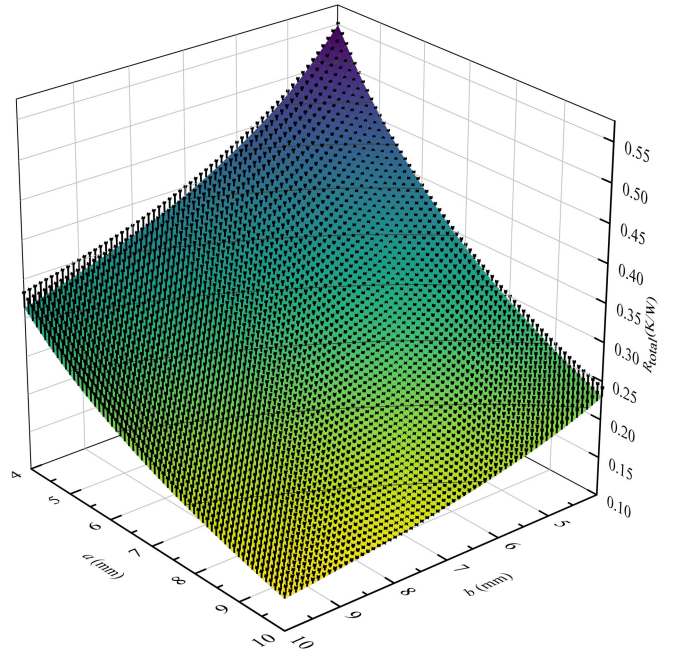


Fig. 9. Effect of different chip sizes.

the chip's aspect ratio is below 1.28 (e.g., $a = 4$ mm and $b = 6.5$ mm), whereas, for aspect ratios greater than 1.28, the error range is between 1% and 2%, similar to the DBC case.

B. FSS-TRM Validation With CRRC Power Module

In this section, the effectiveness and efficiency of FSS-TRM were tested using a commercial 1.2-kV/50-A 34-mm package module [made by China Railway Rolling stock Corp (CRRC)]. To verify the accuracy and efficiency of the FSS-TRM, we compare the FSS-TRM result with the experimental result, COMSOL, and commonly used thermal resistance calculation methods. First, the power module thermal resistance was measured through experimental methods.

1) *Experimental Test*: The experimental setup for thermal resistance testing is illustrated in Fig. 10. A constant-current

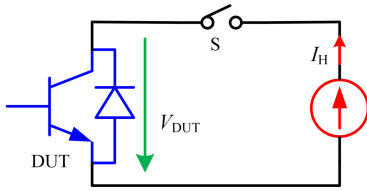


Fig. 10. Thermal resistance testing circuit schematic.

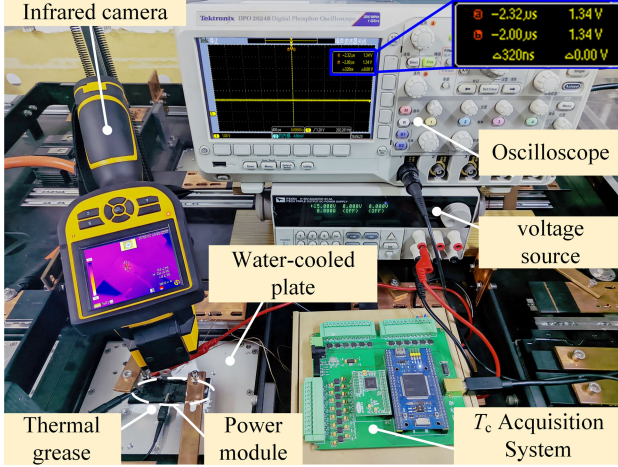


Fig. 11. Experimental platform for thermal resistance testing of the power module.

source is applied to the device under test (DUT) using a switch (S) to regulate the heating time. Once S is closed, the temperatures of both the DUT's junction and case are recorded, along with the saturation voltage of DUT (V_{DUT}), once they have reached a steady state. Consequently, the steady-state heating power of the DUT can be obtained, expressed as $P_H = V_{DUT} \cdot I_H$. From this, the thermal resistance of the power module can be derived.

A thermal resistance testing platform was constructed to experimentally verify TPPM, as illustrated in Fig. 11. The module case temperature was measured using a K-type thermocouple, and an infrared camera was used to measure the chip's junction temperature. To ensure the stable operation of the module, a water-cooling plate was connected to the power module baseplate via thermal grease. Notably, the module was not encapsulated, allowing for direct measurement of the chip's junction temperature but introducing nonunique heat dissipation paths. To rectify this issue, the module surface was sprayed with black paint (emissivity of 0.94) to ensure a single path for heat dissipation. The DUT was kept open using a 15-V voltage source, while a current source supplied 20 A to heat the DUT.

A well-designed experimental scheme was conducted to ensure the accuracy and reliability of the experimental data. First, the chip diagonal was chosen as the capture area, and three temperature measurement points were evenly arranged within this area to obtain the average chip junction temperature. At the same time, a K-type thermocouple was employed to measure the module case temperature. Second, the infrared camera collected multiple sets of chip junction temperature data at different case temperatures during the experiment, as depicted in Fig. 12.

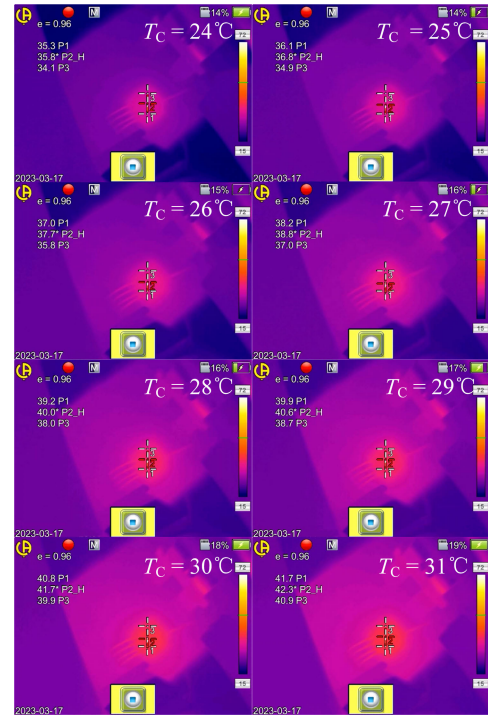


Fig. 12. Junction temperature collected by the infrared camera under different test conditions.

 TABLE I
 CRRC POWER MODULE EXPERIMENTAL TEST DATE

Test	T_c ($^{\circ}\text{C}$)	T_j ($^{\circ}\text{C}$)			\bar{T}_j ($^{\circ}\text{C}$)	R (K/W)
		1	2	3		
1	24	35.3	35.8	34.1	35.067	0.413
2	25	36.1	36.8	34.9	35.933	0.408
3	26	37.0	37.7	35.8	36.833	0.404
4	27	38.2	38.8	37.0	38.000	0.410
5	28	39.2	40.0	38.0	39.067	0.413
6	29	39.9	40.6	38.7	39.733	0.400
7	30	40.8	41.7	39.3	40.600	0.396
8	31	41.7	42.3	40.9	41.633	0.397

 TABLE II
 MATERIAL PROPERTIES AND THICKNESS PARAMETERS
 OF THE POWER MODULE PRODUCED BY CRRC

Material	Chemical formula	Thickness (mm)	Thermal conductivity $\text{W}/(\text{m} \cdot \text{K})$	Heat capacity $\text{J}/(\text{kg} \cdot \text{K})$	Density (kg/m^3)
Die solder	Sn95Ag5	0.1	20	306	7400
The DBC top side	Cu(1920)	0.3	300	385	8930
Ceramics	Al_2O_3	0.6	24	765	3260
The DBC bottom side	Cu(1920)	0.3	300	385	8930
Baseplate solder	Sn95Ag5	0.1	20	306	7400
Baseplate	Cu15Mo85	3.0	160	385	8930

It is worth mentioning that all experimental data presented in this article were obtained under steady-state conditions. First, V_{DUT} was measured as 1.34 V using an oscilloscope, and the heating power of the DUT was calculated as 26.8 W. Subsequently, the thermal resistance of the power module was measured under various test conditions, as summarized in Table I. Finally, the thermal resistance obtained from the experimental testing was expressed as the average thermal resistance over the eight different test conditions. The results indicate that the thermal resistance of the power module is 0.405 K/W.

TABLE III
COMPARISON OF FSS-TRM WITH COMMON THERMAL RESISTANCE CALCULATION METHODS (TEST COMMERCIAL 34-mm PACKAGE POWER MODULE MADE BY CRRC)

Method	Principle	Software	Heat spreading angle (°)	Speed (s)		R (K/W)	Error (%)
				Mesh	Solution		
3D	FEM	COMSOL	-	81.9	164	0.405	0
[30]			0	0	1.1×10^{-4}	0.064	84.2
[18]			30	0	1.9×10^{-4}	0.154	62.0
[19]	$R = \sum_{i=1}^7 t_i / (k_i A_i)$	MATLAB	45	0	2.2×10^{-4}	0.194	52.2
[21]			Inverse tangent of the thermal conductivity	0	4.0×10^{-4}	0.333	17.9
[20]			Tangent of the thermal conductivity	0	4.2×10^{-4}	0.344	15.1
FSS-TRM	Eq.(19) and (24)	MATLAB	-	0	2.8×10^{-3}	0.409	0.9

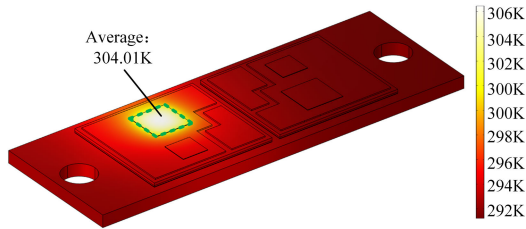


Fig. 13. FEM thermal resistance testing in CRRC power module.

2) *Common Methods Test*: To validate the computational efficiency and accuracy of FSS-TRM, we conducted a comparative analysis using various commonly employed thermal resistance calculation methods to evaluate the thermal resistance of a commercial 34-mm package power module. This investigation was conducted using MATLAB 18a and COMSOL 5.6, running on an Intel¹ Core i7-10700F CPU with 32-GB RAM.

First, this study employs COMSOL to establish the geometric model of a 34-mm package module (made by CRRC). Since bonding wires have a negligible impact on thermal simulation results [29], they are not included in the model. The material properties and thickness parameters of the module are provided in Table II. The module baseplate is set to a 293.15-K isothermal surface to simulate experimental conditions, and the chip power loss is set to 26.8 W. The results in Fig. 13 indicate a thermal resistance of 0.405 K/W.

Table III shows that traditional calculation methods enhance the accuracy of thermal resistance calculations by refining the precision of heat transfer area considerations. However, despite their notable computational efficiency, even the most recent evaluation methods exhibit prediction errors exceeding 15%.

In contrast, FSS-TRM obviates the need for precise heat transfer area considerations. While the computational time required by FSS-TRM surpasses that of conventional methods by order of magnitude, its computational accuracy is amplified by two orders of magnitude, resulting in a computational error of less than 1%.

Compared with FEM, FSS-TRM simplifies thermal evaluation by eliminating 3-D modeling and requiring only input parameters (geometric dimensions and thermal parameters).

Despite introducing a 0.9% error, FSS-TRM's computational time reduction by five orders remains acceptable.

The thermal resistance of a commercial 34-mm packaging module (manufactured by CRRC) was assessed using these methods. In COMSOL and experimental testing, the thermal resistance is 0.405 K/W, while in FSS-TRM testing, the thermal resistance is 0.409 K/W. However, the experimental testing method is unsuitable for power module thermal design. Although COMSOL provides high accuracy, it demands substantial computational resources and time. Other computational methods (as discussed) have significant errors, despite computational efficiency. Conversely, FSS-TRM, while having a 0.9% margin of error, reduces computation time by five orders of magnitude compared with COMSOL. These results demonstrate that FSS-TRM is an efficient and accurate method for evaluating TPPM.

C. FSS-TRM Validation Using Several Commercial Power Modules

In this section, the FSS-TRM generality was validated using commercial power modules from different manufacturers. Specifically, we selected 1.2-kV/75-A 34-mm packaged IGBT powers manufactured by Build Your Dreams (BYD) and YangJie companies. Experimental conditions, data processing, and methodologies mirrored those detailed in Section IV-B. Detailed experimental results are presented in Fig. 14.

The DUT was maintained open with a 15-V voltage source, while a 20-A current source was employed for DUT heating. Beginning with the BYD power module, V_{DUT} was measured at 1.90 V, and the heating power of the DUT was calculated at 38.0 W. Simultaneously, measurements for the YangJie power module indicated V_{DUT} of 1.63 V, corresponding to a heating power of 32.6 W. Furthermore, thermal resistance predictions were performed for both modules using FSS-TRM, and the error between FSS-TRM and the experimental tests was computed. Comprehensive experimental data are provided in Table IV.

By evaluating the thermal resistance of power modules produced by CRRC, BYD, and YangJie using the FSS-TRM, the errors were 0.9%, 0.55%, and 0.24%, respectively. This research confirms the effectiveness of FSS-TRM in assessing the power modules' thermal resistance. In summary, the

¹Registered trademark.

TABLE IV
COMPARING FSS-TRM WITH EXPERIMENTAL METHODS: TESTING MODULES PRODUCED BY BYD AND YANGJIE

Company	Test	T_c (°C)	T_j (°C)			\bar{T}_j (°C)	R (K/W)	\bar{R} (K/W)	FSS-TRM (K/W)	Error (%)
			1	2	3					
BYD	1	24	36.2	38.7	38.4	37.767	0.362	0.364	0.362	0.55
	2	25	37.6	39.6	38.7	38.633	0.359			
	3	26	39.0	40.7	40.1	39.933	0.367			
	4	27	39.5	41.4	41.1	40.667	0.360			
	5	28	40.9	42.5	42.4	41.933	0.367			
	6	29	42.2	43.4	43.2	42.933	0.367			
	7	30	43.7	44.4	43.6	43.900	0.366			
	8	31	44.4	45.5	44.9	44.933	0.367			
YangJie	1	24	37.1	38.0	37.1	37.400	0.411	0.415	0.416	0.24
	2	25	38.2	39.2	38.2	38.533	0.415			
	3	26	39.3	40.3	39.3	39.633	0.418			
	4	27	40.3	41.3	40.4	40.667	0.419			
	5	28	41.2	42.2	41.2	41.533	0.415			
	6	29	42.3	43.1	42.1	42.500	0.414			
	7	30	43.3	44.2	43.1	43.533	0.415			
	8	31	44.3	45.2	44.0	44.500	0.414			

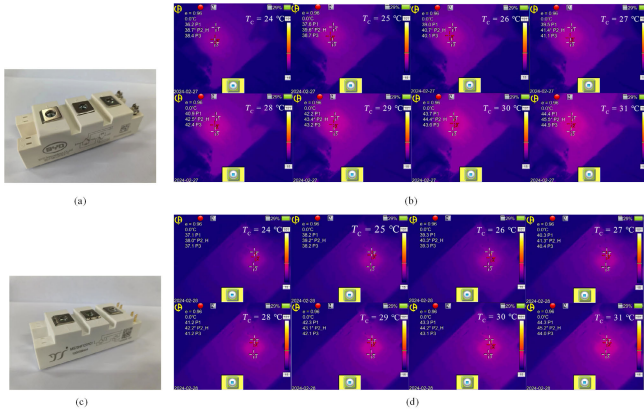


Fig. 14. Experimental thermal resistance testing of various power modules. (a) Power module made by BYD. (b) Junction temperature testing for BYD power module. (c) Power module made by YangJie. (d) Junction temperature testing for YangJie power module.

proposed FSS-TRM is suitable for thermal resistance assessment in power modules, offering minimal evaluation errors (less than 1%) and rapid assessment speed (completed within milliseconds). Therefore, it could shorten the development cycle of power module thermal design.

V. CONCLUSION

This article proposes a novel FSS-TRM method for estimating the TPPM with improved efficiency and accuracy. Experimental and COMSOL results confirm that the thermal resistance obtained from FSS-TRM closely matches that of the 34-mm package power module. This method offers a relatively simple approach for accurately calculating the thermal resistance of power modules and optimizing their layout and structure in thermal design. Unlike traditional methods, the FSS-TRM does not require constructing a physical geometry model or calculating the temperature field of the entire power module, simplifying the estimation process. Furthermore, while the FSS-TRM uses a single heat source to calculate

thermal resistance, it can efficiently evaluate the thermal performance of multichip power modules by adding the resistance generated by the FSS-TRM to the coupled thermal resistance, as has been extensively studied in previous research.

Currently, thermal coupling problems are mainly addressed using coupled thermal resistance. However, this model provides an abstract description of the thermal behavior and lacks a comprehensive analysis and description of the thermal coupling problem in multichip power modules. Therefore, describing thermal coupling in multichip modules will be a key future research direction. In addition, constructing a physical model using mathematical–physical methods to understand thermal coupling presents an intriguing avenue of study accurately. Such a model would offer novel design ideas for thermal management and provide a new approach for thermal performance evaluation in multichip power modules.

APPENDIX

FOURIER COEFFICIENT CALCULATION

Before calculating the Fourier coefficients, it is necessary to analyze the boundary conditions. In this analysis, the first step is to calculate the partial derivative of (13) in the z -direction

$$\begin{aligned}
 \frac{\partial \theta_i}{\partial Z} = & B_i \\
 & + \sum_{m=1}^{\infty} \cos(\alpha_m x) [A_{i,m} \alpha_m \sinh(\alpha_m z_i) \\
 & + B_{i,m} \alpha_m \cosh(\alpha_m z_i)] \\
 & + \sum_{n=1}^{\infty} \cos(\beta_n y) [A_{i,n} \beta_n \sinh(\beta_n z_i) + B_{i,n} \beta_n \cosh(\beta_n z_i)] \\
 & + \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \cos(\alpha_m x) \cos(\beta_n y) [A_{i,mn} \gamma_{mn} \sinh(\gamma_{mn} z_i) \\
 & + B_{i,mn} \gamma_{mn} \cosh(\gamma_{mn} z_i)]. \tag{A-1}
 \end{aligned}$$

The Fourier series-based function, as indicated by expression (A-1), incorporates coefficients A_i and B_i . This section will be divided into two parts to provide a detailed process for solving the coefficients. The solution procedure for the coefficient B_i is first shown in the following discussion.

A. Solution for B_i

It is important to obtain the expression of the coefficient (A_i and B_i) for the expression based on the Fourier series. Consequently, this part provides a comprehensive account of the determination of the B_i coefficient. It should be noted that when h is sufficiently large, T_c can be approximated by T_f , and thus, the junction-to-case temperature can be effectively represented by θ_1 . This means that only B_1 coefficients must be solved. Hence, (A-1) can be written as follows:

$$\begin{aligned} \left. \frac{\partial \theta_1}{\partial z} \right|_{z=0} &= B_1 \\ &+ \sum_{m=1}^{\infty} B_{1,m} \alpha_m \cos(\alpha_m x) \\ &+ \sum_{n=1}^{\infty} B_{1,n} \beta_n \cos(\beta_n y) \\ &+ \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} B_{1,m,n} \gamma_{1,m,n} \cos(\alpha_m x) \cos(\beta_n y). \quad (\text{A-2}) \end{aligned}$$

According to (A-2), the solving process for $B_{1,m}$, $B_{1,n}$, and $B_{1,mn}$ is similar. In addition, all B_1 can be obtained using (4). Therefore, the Fourier transform of (4) in the x -direction can be expressed in the following form:

$$\begin{aligned} &\int_0^{L_x} \int_0^{L_y} \left(\sum_{m=1}^{\infty} B_{1,m} \alpha_m \cos(\alpha_m x) \right) \cos(\alpha_m x) dx dy \\ &= \int_{Y_c - \frac{b}{2}}^{Y_c + \frac{b}{2}} \int_{X_c - \frac{a}{2}}^{X_c + \frac{a}{2}} \left(-\frac{Q}{4A_s k_1} \right) \cos(\alpha_m x) dx dy. \quad (\text{A-3}) \end{aligned}$$

Therefore, the Fourier coefficients can be calculated as follows:

$$B_{1,m} = \sum_{m=1}^{\infty} \frac{-4Q \cos(\alpha_m X_c) \sin(\alpha_m \frac{a}{2})}{L_x L_y a k_1 \alpha_m^2}. \quad (\text{A-4})$$

Similarly, others can be calculated as follows:

$$B_{1,n} = \sum_{n=1}^{\infty} \frac{-4Q \cos(\beta_n Y_c) \sin(\beta_n \frac{b}{2})}{L_x L_y b k_1 \beta_n^2}. \quad (\text{A-5})$$

$$\begin{aligned} B_{1,m,n} &= \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \frac{-16Q \cos(\alpha_m X_c) \sin(\alpha_m \frac{a}{2})}{L_x a k_1 \alpha_m} \\ &\times \frac{\cos(\beta_n Y_c) \sin(\beta_n \frac{b}{2})}{L_y b \beta_n \gamma_{mn}}. \quad (\text{A-6}) \end{aligned}$$

B. Solution for A_i

Similar to the above solution process, a calculation process in the x -direction is noted. By substituting (A-1) into (5), it can be expressed as follows:

$$\begin{aligned} &k_i [A_{i,m} \sinh(\alpha_m z_i) + B_{i,m} \cosh(\alpha_m z_i)] \\ &= k_{i+1} [A_{i+1,m} \sinh(\alpha_m z_i) + B_{i+1,m} \cosh(\alpha_m z_i)]. \quad (\text{A-7}) \end{aligned}$$

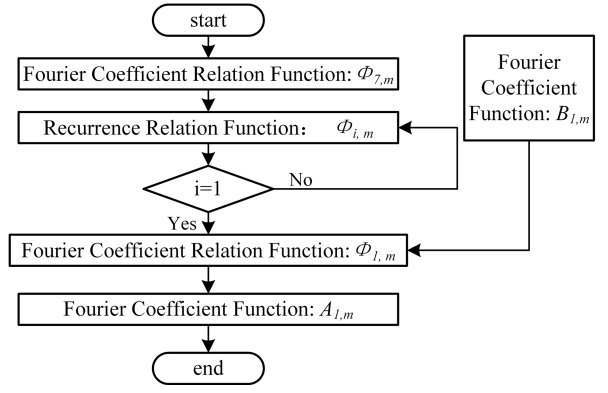


Fig. 15. Solution process of Fourier coefficient $A_{1,m}$.

By substituting (13) into (6), it can be written as follows:

$$\begin{aligned} &A_{i,m} \cosh(\alpha_m z_i) + B_{i,m} \sinh(\alpha_m z_i) \\ &= A_{i+1,m} \cosh(\alpha_m z_i) + B_{i+1,m} \sinh(\alpha_m z_i). \quad (\text{A-8}) \end{aligned}$$

Then, (A-7) \times $\cosh(\alpha_m z_i)$ and (A-8) \times $\sinh(\alpha_m z_i)$ can be written as follows:

$$\begin{aligned} B_{i+1,m} &= -\{A_{i,m} \sinh(\alpha_m z_i) \cosh(\alpha_m z_i) (1 - K) \\ &+ B_{i,m} [\sinh^2(\alpha_m z_i) - \cosh^2(\alpha_m z_i) K]\} \quad (\text{A-9}) \end{aligned}$$

where $K = k_i/k_{i+1}$.

Equations (A-8) \times $\cosh(\alpha_m z_i)$ and (A-7) \times $\sinh(\alpha_m z_i)$ can be written as follows:

$$\begin{aligned} A_{i+1,m} &= A_{i,m} [\cosh^2(\alpha_m z_i) - K \sinh^2(\alpha_m z_i)] \\ &+ B_{i,m} \sinh(\alpha_m z_i) \cosh(\alpha_m z_i) (1 - K) \quad (\text{A-10}) \end{aligned}$$

where i from 1 to 6 in (A-7)–(A-10). Define the relationship between $A_{i,m}$ and $B_{i,m}$ as follows:

$$\Phi_{i,m} = -\frac{B_{i,m}}{A_{i,m}}. \quad (\text{A-11})$$

Thus, the recurrence relation for $\Phi_{i,m}$ can be obtained from (A-9) and (A-10) as (A-12), as shown at the top of the next page.

According to above calculation, to successfully obtain the formula of $A_{1,m}$, $\phi_{7,m}$ is key issue that will be calculated next. By substituting (13) and (A-1) into (8), it can be expressed as follows:

$$\begin{aligned} &K_7 [A_{7,m} \alpha_m \sinh(\alpha_m z_N) + B_{7,m} \alpha_m \cosh(\alpha_m z_N)] \\ &= -h [A_{7,m} \cosh(\alpha_m z_N) + B_{7,m} \sinh(\alpha_m z_N)]. \quad (\text{A-13}) \end{aligned}$$

Simplifying (A-13) yields

$$\Phi_{7,m} = \frac{h \cosh(\alpha_m z_7) + K_7 \alpha_m \sinh(\alpha_m z_7)}{h \sinh(\alpha_m z_7) + K_7 \alpha_m \cosh(\alpha_m z_7)}. \quad (\text{A-14})$$

With the above calculation, the Fourier coefficients of all summation terms can be obtained. To better represent the process, a flowchart is presented in Fig. 15.

$$\Phi_{i,m} = \frac{\Phi_{i+1,m} [\cosh^2(\alpha_m z_i) - K \sinh^2(\alpha_m \cdot z_i)] - \sinh(\alpha_m \cdot z_i) \cosh(\alpha_m \cdot z_i)(1 - K)}{\Phi_{i+1,m} \sinh(\alpha_m \cdot z_i) \cosh(\alpha_m \cdot z_i)(1 - K) - [\sinh^2(\alpha_m z_i) - \cosh^2(\alpha_m \cdot z_i)K]} \quad (\text{A-12})$$

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