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A Review of Graphene-Based Memristive Neuromorphic Devices and Circuits

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As data processing volume increases, the limitations of traditional computers and the need for more efficient computing methods become evident. Neuromorphic computing mimics the brain's low-power and high-speed computations, making it crucial in the era of big data and artificial intelligence. One significant development in this field is the memristor, a device that exhibits neuromorphic tendencies. The performance of memristive devices and circuits relies on the materials used, with graphene being a promising candidate due to its unique properties. Researchers are investigating graphene-based memristors for large-scale, sustainable fabrication. Herein, progress in the development of graphene-based memristive neuromorphic devices and circuits is highlighted. Graphene and its common fabrication methods are discussed. The fabrication and production of graphene-based memristive devices are reviewed and comparisons are provided among graphene- and nongraphene-based memristive devices. Next, a detailed synthesis of the devices utilizing graphene-based memristors is provided to implement the basic building blocks of neuromorphic architectures, that is, synapses, and neurons. This is followed by reviewing studies building graphene memristive spiking neural networks (SNNs). Finally, insights on the prospects of graphene-based neuromorphic memristive systems including their device- and network-level challenges and opportunities are given.

1. Introduction

Electronics and computer engineers and scientists are always looking to further improve computers and computing methods. Neuromorphic computing is a branch of engineering that aims to replicate the low power, highly parallel, and high throughput of the brain, which is one of the most highly efficient and powerful computers known to exist.[1] Key to any neuromorphic architecture, such as the spiking neural network (SNN), is the utilization of event-driven, asynchronous voltage spikes. Using these spikes significantly reduces the power consumption of these networks compared to traditional deep neural networks (DNNs).[2,3]

Neuromorphic networks are designed using two fundamental building blocks; neurons and synapses, which are represented in the top panel of **Figure 1**. The neurons, in their simplest integrate and fire form, are designed to take weighted summations of their input to generate an output (middle panel of Figure 1). In neuromorphic structures, the inputs can be represented in the form of voltage spikes, which represent events presented to the system for processing, or information to transfer across the network. In this widely accepted form, these spikes are added to the neuron's membrane potential until a given threshold is reached, where an output spike is generated and the membrane potential is reset.

The second fundamental neuromorphic building block is the synapse. The synapse acts as the place where the weight of the input (referred to as the synaptic weight) is stored and modified (see the middle panel of Figure 1). Various learning rules can be applied at the synapse, all with different benefits and drawbacks. In SNNs, common learning rules include rate-based rules such as spike-rate-dependent plasticity (SRDP) and time-based rules such as spike-timing-dependent plasticity (STDP). SRDP compares the firing rates of input and output to determine the change in the synaptic weight, while STDP relates the timing of pre- and postsynaptic spikes to govern the change in the synaptic weight. Implementing these learning rules and the neuronal integrate and fire behavior can be efficiently realized by utilizing specific devices known as memristors.[4]

Memristors are two terminal devices that effectively act as resistors with a form of memory. First proposed by Leon Chua in 1971,[5] the link between thin-film resistive switching (RS) devices and the memristor was first established in 2008.[6] Since then, memristor research has exploded, with many devices having been fabricated and tested for their neuromorphic applications.[4] Memristors are particularly advantageous to use because they can eliminate what is known as the von Neumann bottleneck, caused by the separation of processing and memory elements in traditional computing architectures.[7] As

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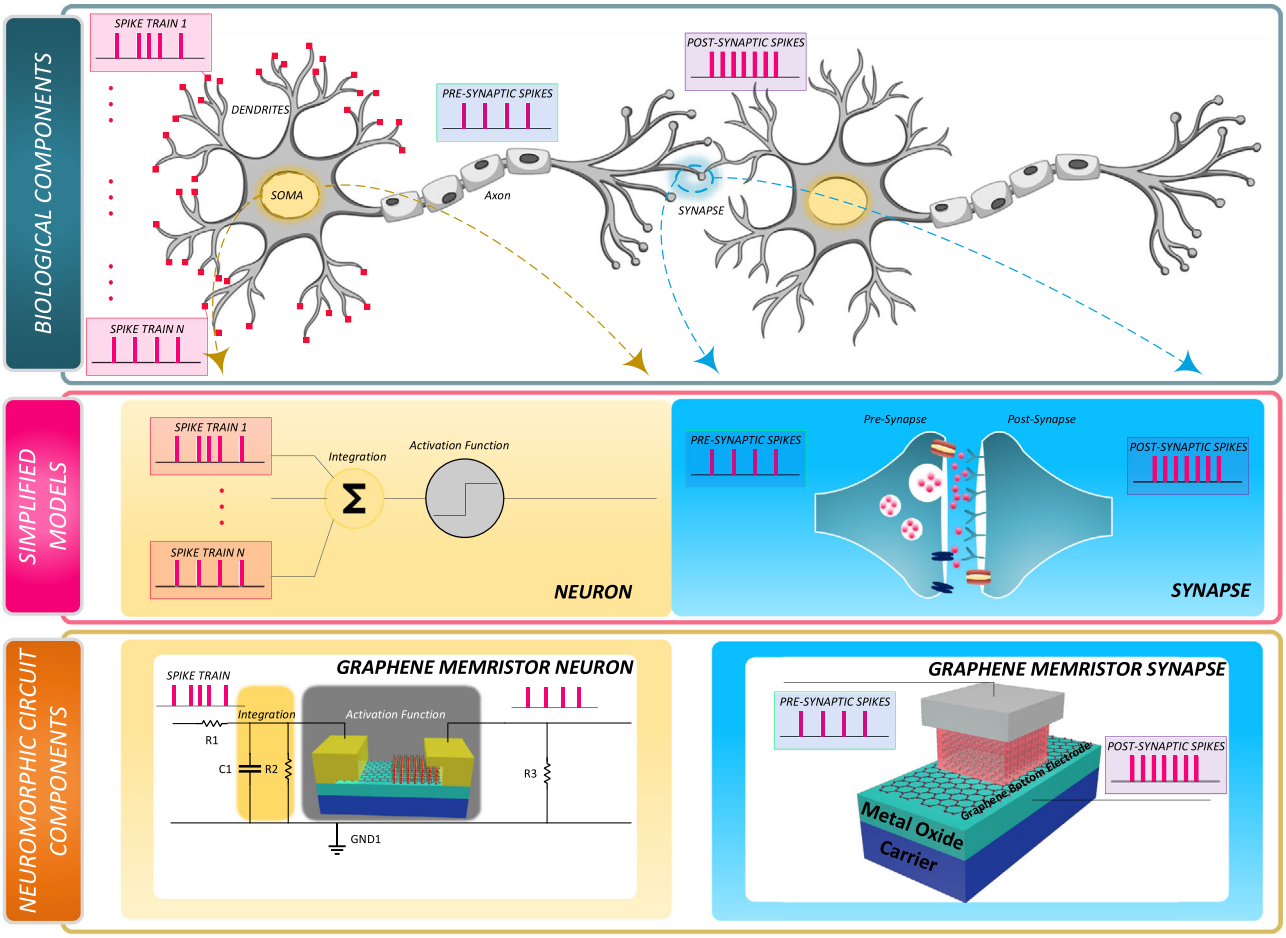

Figure 1. Utilizing graphene-based memristive devices in neuromorphic settings. The general structure of biological components (i.e., neurons and synapses) and their connectivity is illustrated in the top panel. The middle panel demonstrates simplified models of the biological neuron and synapse. Here, the soma of the neuron (yellow) is modeled with a summation term and an activation function, while the synapse structure visualizes the neurotransmitters and neuroreceptor mechanism. The bottom panel shows simplified equivalent graphene-based memristive neuromorphic circuits for the simplified models. Here, part of the neuron is a transistor structure composed of graphene at its gate (similar to the design in ref. [58]), implementing the activation function of the model neuron. The synapse is a sandwich filament-based memristive structure showing graphene at its bottom electrode.

memristors are able to simultaneously change and store their conductance, they could significantly improve the efficiency and performance of future computers by performing computations in the place of memory, i.e., in-memory computing (IMC).[8]

Due to their IMC feature, memristors are often used for neuromorphic synaptic applications.[7,9] As shown in the bottom right panel of Figure 1, memristors are often placed as a direct substitute for the synapse. The synaptic weight is then stored in the conductance of the memristive device, which can be altered using various learning mechanisms. Another application of memristors in neuromorphic computing is in neuronal circuits. As shown in the bottom left panel of Figure 1, the memristor plays an important role in the output spiking of a memristive neuron. Here, the resistor–capacitor circuit is responsible for the temporal integration of the incoming voltage spikes. When the capacitor is sufficiently charged, the memristor undergoes an increase in conductance, producing output spikes. Hence, memristors pose as ideal candidates for investigating neuromorphic applications.

In addition to their spiking neuromorphic applications, memristor's IMC abilities have been widely studied in conventional, non-SNNs and machine learning. Furthermore, memristors made from organic materials have similar properties to organic processing units such as the eye or skin.[10] As such, areas such as visual processing and storage,[11] tactile perception,[12] and auditory processing[13] can all be implemented using memristive devices.[14] Furthermore, by tuning properties such as optical transparency, memristors can serve as image sensors as well. This could be useful for neuromorphic applications as neuromorphic computing benefits from event-based data. As such, designing sensing systems that can collect data in a neuromorphic way is tailored for neuromorphic systems. Despite the many interesting applications, in this article, we focus mainly on the use of memristors in spiking neuromorphic architectures.

The materials used to manufacture memristive devices play a significant role in their performance, cost, and environmental impact. One material of particular interest is graphene, due to its superior electrical, mechanical, and thermal properties, which can be recently achieved through sustainable fabrication methods.[15–18] Due to these benefits, graphene-based memristive neuromorphic components (see the bottom panel of Figure 1) have attracted high research and development interests.

In this article, we will discuss graphene, and how it can be utilized to build memristive devices that can be implemented into various neuromorphic architectures. Section 2 will outline the various properties, fabrication processes, and applications of graphene. Section 3 will cover the literature on different graphene-based memristive devices that have been developed. Section 4 will discuss the various synapses and synaptic structures that have been developed using graphene memristive devices. For this section, only devices that were characterized to perform a spike-based learning rule were considered, due to our paper's neuromorphic focus. Section 5 will discuss the various neuronal circuits that have been developed using graphene-based memristive devices. Section 6 will provide an overview of the various neuromorphic networks that have utilized graphene-based devices. Section 7 provides insights into the challenges and opportunities of using graphene-based memristors in neuromorphic computing, while Section 8 concludes the paper.

2. Graphene

2.1. Properties of Graphene

Although graphene simply consists of a single layer of carbon atoms bonded together, its prospects and future in electrical engineering is unlike any other material. A list of graphene's superior electrical properties includes zero bandgap, a linear energy dispersion near the Dirac point, and a high electron mobility of $15\,000\,cm^2V^{-1}s^{-1}$.[19] This high electron mobility means that graphene has an extremely high in-plane conductivity at room temperature, while its through-plane conductivity is more comparable to an insulator. Optically, graphene is mostly transparent and only absorbs 2.3% of incoming white light.[20] Furthermore, the optical absorption of graphene is independent of wavelength,[21] and leads to many useful outcomes such as two-photon absorption, four-wave mixing, and a saturable absorber.[21]

To add to this, graphene is also known to possess a large thermal conductivity, which varies between 3000 and $5000\,W\,mK^{-1}$ at room temperature.[22] A high thermal conductivity suggests that graphene can act as a heat sink. Furthermore, due to its strong anisotropy brought about by its structure, graphene's through-plane thermal conductivity is much lower, because it is limited by the weak van der Waals interactions between substrates,[22] which suggests potential implementation for thermal insulation as well. Additionally, graphene is known to be mechanically robust, making it suitable for applications requiring flexibility such as wearable devices.[19]

Graphene's unique properties means many electronic devices could see improvement in the future. This includes devices such as various transistors, transparent conducting electrodes, light-emitting diodes, photovoltaics, and other applications.[19] However, the class of device most relevant for this article is the memristor, and many researchers have developed graphene-based memristive devices. Although other 2D materials such as black phosphorous, boron nitrides, dichalcogenides, and 2D perovskite have also picked up interest in this field,[23–26] in this literature review, we merely focus on graphene-based memristive devices.

2.2. Motivation for Using Graphene

As mentioned in the previous section, graphene has a wide range of properties suitable for a variety of applications. For neuromorphic applications like SNNs, the memristor serves as a promising candidate to perform IMC and significantly accelerate performance. Hence, utilizing graphene's properties in memristive devices can lead to many advances, such as flexible memristive devices,[26] low power devices[27] and memristive devices with optical applications.[28]

However, this is not the only motivation for using graphene. The methods used to fabricate graphene play a significant role in its commercial viability and its environmental sustainability. Currently, there is a need for graphene to be produced at a low cost, in large volumes, and in a sustainable manner. In a previous work,[17] we used the plasma-enhanced chemical vapor deposition (PECVD) method to fabricate graphene, without using a catalyst, and by using *Melaleuca alternifolia* (a natural extract from the tea-tree plant) as the precursor. Our work demonstrated that high-quality graphene can be fabricated using this sustainable technique, further showing the benefits of utilizing graphene for memristive device fabrication in neuromorphic applications.

Works such as refs. [29,30] have also demonstrated promising and sustainable methods of graphene production. In ref. [29], an environmentally benign method of producing few layer graphene was reported. George et al. exfoliated graphene using naturally available phenolics. In ref. [30], epitaxial growth was used to fabricate wafer-sized, single-crystal graphene. This method had the advantages of wafer compatibility, fast (≈10 min) production, and excellent scalability.

2.3. Graphene Fabrication Methods

The first work detailing a method for fabricating graphene was published in 2004.[31] Interestingly, the graphene was produced by removing the surface layer graphene from graphite using tape.[32] The graphene flakes of varying thicknesses could reach up to 1 mm in size.[31] Other mechanical exfoliation methods include using atomic force microscope tips to extract the surface layer,[33] and it has been found that a force of $300\,nN\,\mu m^{-2}$ is required to separate the surface graphite. However, mechanical exfoliation is limited by its inability to be scaled and reproduced in a consistent manner.

As more research has been developed for graphene and graphene-based memristive devices, many other methods of production have come to light, such as epitaxial growth,[34–36] chemical exfoliation,[37–39] unzipping carbon nanotubes,[40–42] and other methods.[43] One of the most promising methods

for producing large volumes of high-quality graphene is chemical vapor deposition (CVD). This bottom-up method requires gaseous reactants to undergo chemical reactions to deposit solids onto various substrates.[44] The CVD method has been used to produce graphene in many different works;[45–47] however, this method has some potential drawbacks as well. Often, CVD requires high temperatures and pressures to deposit graphene onto a substrate.[33] A variation of the CVD is the PECVD method, where the gases react in the presence of a plasma, which can lower the required temperatures and pressures. The plasma can be induced via radio frequency (RF), microwave or inductive coupling. Many works have demonstrated graphene fabrication using this method.[17,48–50]

Epitaxial growth is also a method that allows the deposition of a single-crystalline film (epitaxial film) on a single-crystal substrate. Although lesser studied than CVD, epitaxial growth of graphene is still quite common,[35,36] due to scalability, high-quality product, and exceptional electronic properties. However, one of the drawbacks of epitaxial growth is the substrate used. Metal substrates are suitable for epitaxial growth of graphene, however, for electronics applications such as neuromorphic computing, it is much more suitable for growth to occur on an insulator. Hence, an alternative such as SiC is used instead. However, SiC suffers from drawbacks such as limited quality due to the inability to control sublimation rates at temperatures between 900 and 1300 °C and that thermal decomposition is limited to the use of 3C–SiC (111) surface.[51]

3. Graphene-Based Memristors

Memristors are two terminal devices that are set to change the dynamics of computing. First proposed in ref. [5] as a fourth, fundamental electrical component, the fabrication, characterization, and implementation of memristors have seen a huge interest from electronic and material engineering researchers. Memristive devices have the unique property where the conductance/resistance of the device is dependent on previously applied voltages and currents, allowing the devices to possess a form of memory in their conductive/resistive state (and hence the term "mem"-"ristor"). Utilizing the conductance in this way is said to provide many benefits, including overcoming the von Neumann bottleneck and lower power and area consumption.[4,7] This section will cover the various graphene-based memristive devices that have been previously developed.

3.1. Graphene-Based Memristor Fabrication Methods

When manufacturing graphene-based memristive devices, graphene is often grown using CVD.[52–54] This is largely owing to this method's potential to fabricate high-quality graphene in large volumes, at a relatively cost-effective rate. To build graphene-based memristive devices, graphene is often synthesized and then transferred to the device, or the materials of the device are deposited on top of the graphene via thermal evaporation or other techniques. In limited cases, other methods have been used. This is the case in works such as,[55] where graphene was grown using epitaxial growth. In ref. [56], mechanical exfoliation was used to produce a graphene/MoS_2/graphene memristive device. However, these methods are often not considered unless they are required for specific reasons such as fabricating memristive devices with specific materials/needs. Chemical methods, such as those outlined in ref. [57] have also been used to produce graphene oxide for memristive devices, and in some cases such as refs. [26,58], commercially grown graphene has been used to fabricate the memristive device.

Some studies have investigated unique methods of fabricating graphene-based memristors. In ref. [59], SiO_x memristive nanodots were developed on graphene electrodes via a block copolymer self-assembly process. The cost-effective, scalable, and high resolutions achieved using block copolymer processes can surpass the limits imposed using optical lithography.[59,60] Other interesting methods have also been explored for developing graphene-based memristive devices. The work proposed in ref. [61] investigated inkjet-printed memristors with graphene oxide layers. Printed memristors tend to be larger, on the order of μm as opposed to nm.[62] However, printed memristors can be produced rapidly, at low cost and with minimal waste, making them suitable for rapid prototyping.

3.2. Memristor's Characteristics

When designing memristors, there are a series of parameters that determine the device's suitability for various applications. This includes R_{Off}/R_{On} (or high-resistance state (HRS)/low-resistance state (LRS)) ratio, number of states, switching energy and speed, device size, endurance, retention, and cycle-to-cycle (CTC) and device-to-device (DTD) variability.[4] The R_{Off}/R_{On} is a ratio between the minimum and maximum values of resistance for the memristive device, which is important for distinguishing between states and establishing a dynamic range. The number of states refers to the number of resistance states possible within the memristive device, which is important in determining the possible applications of the device. Switching energy and speed refer to the energy and time required to switch the device from HRS to LRS, respectively. These considerations are important when considering the required power needed to supply the device as well as the maximum speeds that the device can operate under.

Endurance is the property of the memristor to be switched from HRS to LRS consistently, and is measured by the number of cycles of switching from HRS to LRS until state degradation is observed.[63] Retention is the time that a memristor can retain its resistive state before changing state.[63] Finally, the CTC and DTD variations refer to the probabilistic variations in the resistive state (or other properties) as a result of intrinsically stochastic device behavior or device defects between devices, respectively. With an understanding of these parameters, many researchers endeavor to utilize different switching mediums and mechanics to improve these parameters. In the following subsections, we discuss four prominent memristive switching mechanisms and explain how graphene has been integrated into them to build improved memristive devices.

3.3. Building Graphene Heteromaterial Interfaces

Before discussing the various RS mechanics of graphene-based memristors, it is important to discuss how graphene interfaces with other materials, as this interface can play a significant role in determining memristive properties such as the conduction mechanism. For example, in ref. [64], it was noted that the Schottky barrier could be modulated by increased donor concentration for their device. As such, a two orders of magnitude increase in resistance was observed, demonstrating the importance of designing interfaces with graphene. In ref. [65], graphene and TiO_x heterojunctions implemented into a memristive device yielded 10^3 power reduction. Furthermore, the tunneling barrier of their graphene–TiO_x was tunable through tuning the barrier width via SET and RESET operations or by altering the quality of the graphene. In ref. [66], it was even observed that the introduction of a Ta–graphene–TaO_5 can alter the types of ions being migrated in the RS medium by inhibiting TaO_x formation. In turn, this can affect the power consumption, variability, and endurance/retention characteristics of the device.

3.4. Graphene-Based Ferroelectric Polarization Memristors

Some devices utilize the reversible electric polarization with a ferroelectric material to produce RS. These devices are often referred to as ferroelectric tunneling junction (FTJ) devices, and a demonstration of how the device switches in response to different input voltages is provided in **Figure 2**. Clearly, by altering the applied voltage, the average barrier height for charge carriers to tunnel through is altered, resulting in a modification to the conductance. The typical minimum switching energy required to alter the conductance of these devices is ≈100 fJ,[67] which is moderate compared to other mechanisms. However, it should be noted that their scalability is limited by the fact that depolarization tends to occur as the device approaches its critical thickness.

In ref. [68], an FTJ device was developed with a graphene electrode. In this work, graphene's superior in-plane conductance was not the sole factor of device improvement. Instead, graphene was used to control the molecular layers at the graphene–ferroelectric interface. They found that when trapping a layer of NH_3 through the transfer phase, the ferroelectric polarization retention time is several days for both polarized states, suggesting a nonvolatile form of memory. Importantly, they found a R_{OFF}/R_{ON} ratio of ≈6000, providing a large conductance range for neuromorphic purposes.

Another similar vein of study is the introduction of graphene to various field effect transistors (FETs). Due to graphene's superior conductivity, it is often introduced in the channel region of the transistor (connecting the drain to the source). Works such as refs. [28,69–72] use graphene-based transistors, that utilize ferroelectric polarization to produce RS. Some works such as

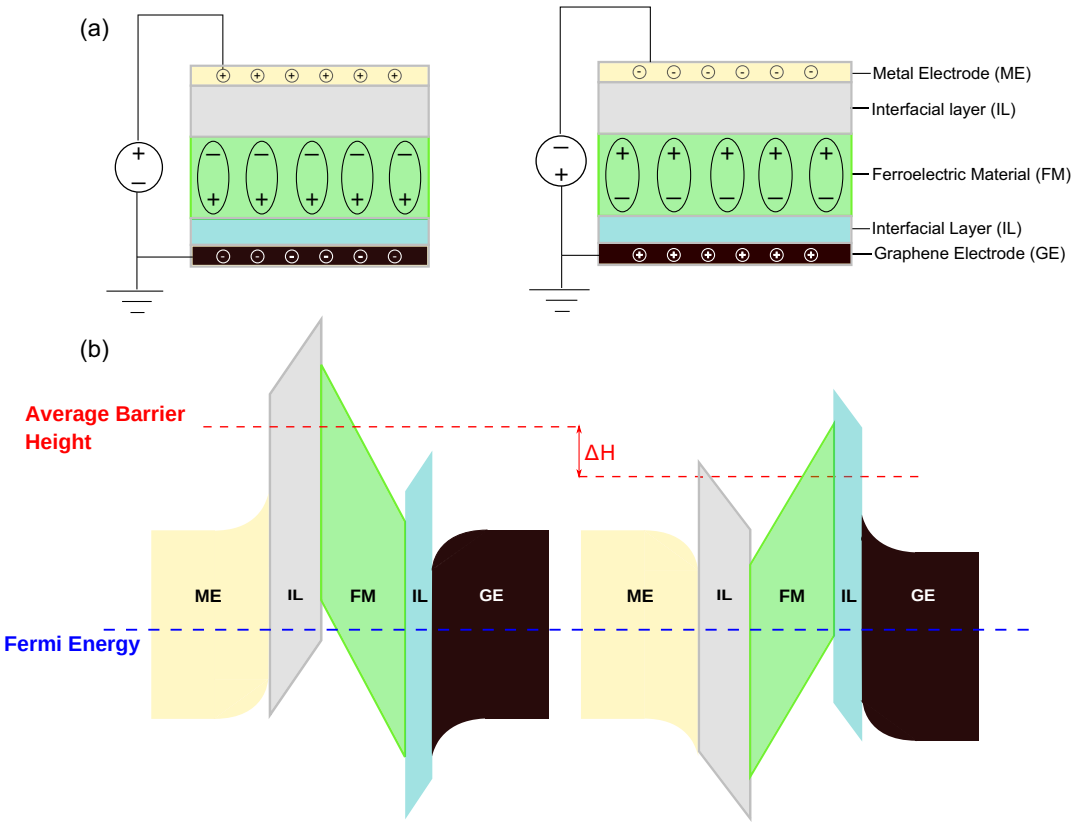

Figure 2. Graphene-based ferroelectric tunneling junction (FTJ) mechanic. a) Illustration of the FTJ mechanic. Note how the polarization within the ferroelectric material changes with the applied voltage. b) The energy band diagrams associated with each polarized state in (a). In this example, the reversal of polarization results in a shift in the average barrier height, resulting in a change in conductance.

refs. [69,72] use the transistor's gate as the third terminal of a memristive device. For instance, Chen et al.[69] utilized this gate to introduce an extra signal which was used to deploy a supervised learning (SL) algorithm.

3.5. Graphene-Based Memristors with Conductive Filament

One of the most common memristive switching mechanics is the formation and rupture of conductive filaments. This is where the electric field applied induces redox reactions within the switching medium that form the conductive filaments. Some filaments are formed through electrochemical metallization (ECM), where an electrolyte is sandwiched between an electrochemically inert electrode such as Pt or Pd and an electrochemically active electrode like Ag[73] or Cu.[74] Some devices utilize valence-change memory (VCM), where oxygen vacancies serve as the conductive filament, and the migration of these ions can be controlled with an applied electric field. For these types of memristors, the electrodes need not consist of active metals; however, they generally possess a longer write/erase endurance cycle due to the lack of impurity residue introduced into the oxide layer, and also because the metal electrode hardly participates in ion migration.[14] In general, conductive filaments have ≈100 fJ switching energy,[67] which is moderate compared to other switching mechanisms.

Investigations surrounding graphene's implementation into conductive filament are often centered around two areas; investigating graphene as an electrode material and investigating graphene oxide as an RS material.[75] Graphene has long been touted as a suitable electrode material for many reasons, including lower power consumption due to high out-of-plane contact resistance, high flexibility, and being used as a blocking layer for atomic diffusion and other effects.[76] As such, graphene can play a useful role for both ECM- and VCM-type devices. For VCM-type devices, graphene (and graphene oxide, a derivative of graphene) play a significant role in the morphology and diffusion of oxygen vacancies,[18,27] whereas for ECM devices graphene can be utilized to limit conductive filament formation for better uniformity and stability,[73,77] as shown in **Figure 3**.

Some examples of graphene-based memristive devices that utilize the conductive filament switching mechanism include.[27,78] The memristive device developed in ref. [27] sandwiches aluminum between aluminum oxide and graphene. Applying various electric fields forms conductive filaments through the migration of oxygen vacancies. The most notable feature about their device is that the switching energy required is less than a femtojoule, which is ideal for power consumption. In ref. [78], graphene and MoS_2 were used to develop a memristor. Both the MoS_2 and the graphene were grown using the CVD method. The monolayer graphene was transferred to a wet p^+ SiO_2/Si substrate, where photolithography was used to pattern the graphene. The graphene then formed the bottom electrode by etching with oxygen plasma. Mo films were then e-beam evaporated onto the etched graphene and then sulfurized using a CVD furnace.

Graphene oxide is another material that is also often investigated for memristor applications. Graphene oxide is a derivative of graphene that consists of a single atomic layer of carbon atoms, but with both surfaces modified by oxygen containing functional groups.[79] Unlike graphene, graphene oxide is hydrophilic, and is easily dispersible in organic solvents,[80] yet is still able to be produced in a similar manner to graphene. Graphene oxide is often investigated as an RS medium, because it shows better RS behavior when used as a dielectric medium compared to graphene. Works such as refs. [80–82] discuss graphene oxide memristive devices, and how graphene oxide contributes to the switching mechanic. Works such as refs. [55,83] have also utilized graphene oxide memristive devices, and have demonstrated the STDP learning rule with their devices.

3.6. Graphene-Based Memristors with Magnetic Tunneling Junction

Magnetic tunneling junction memristors utilize the orientation of the magnetic moment within a material to generate RS, similar to the memristor that utilize the ferroelectric polarization. This type of switching mechanic is less common than others, particularly for when graphene is implemented into the design. This is largely owing to the limited conduction range providing fewer states to manipulate, making them less effective as memristive devices, particularly in neuromorphic environments.[67] Regardless of this, works such as refs. [84,85] have both fabricated graphene-based magnetic tunneling junctions.

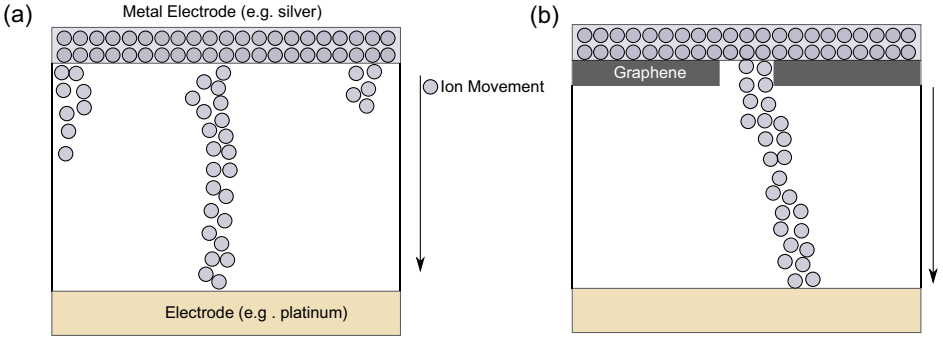

Figure 3. Improving electrochemical metallization (ECM) devices through graphene filament confinement. a) ECM device with no confinement. In this image, multiple filaments are formed, resulting in higher power consumption and a larger degree of variations. b) ECM device with graphene nanohole for filament confinement. Clearly, the graphene limits the migration of metal ions such that only one filament can form.

3.7. Graphene-Based Phase-Change Memory

Phase-change memory (PCM) devices rely on reversible phase changes (induced by joule heating) between an amorphous low conductivity state and a highly conductive crystalline state. Heating the device above the melting temperature of the medium by applying electrical current can alter the device's phase from crystalline to amorphous, which in turn decreases its conductance. Similarly, if the applied current heats the device between the crystallization and melting temperatures, the device re-crystallizes and its conductance is increased. These devices have shown promise for their scalability, however, the phase change requires a significant amount of switching energy, with 1000 fJ being a typical value.[67]

Although graphene has a large in-plane thermal conductivity, it is its low out-of-plane thermal conductivity that is often utilized when developing graphene-based PCM devices. Due to this, graphene often serves as a thermal barrier between the heater electrode and the phase-change material. Doing so confines the heat to a particular region, as shown in **Figure 4**, increasing the temperature of this region without increasing the energy inserted into the device. In ref. [86], graphene was placed as the interface between the $Ge_2Sb_2Te_5$ (GST) and the bottom electrode. In their work, they demonstrated that by introducing graphene, a 40% reduction in the reset current compared to a graphene-free device can be achieved.

Another work that has implemented graphene into a PCM device is ref. [87]. Similar to the work done in ref. [86], they too utilized GST as a PCM material, and demonstrated an 85% reduction in the required reset current in their fabricated device when graphene was introduced. Unlike the previous work, the authors of ref. [87] sandwiched the graphene between a 30 nm thick GST layer and a 10 nm thick GST layer. By applying a 2D finite-element method, they showed that the graphene could confine the heating of the device to the 10 nm GST layer, while increasing the temperature of this area from 740 to 1000 K. Their work also demonstrated that their 40 nm graphene-based device required less reset current than 10 nm devices of the same material, and they attribute this result to the increased series resistance that graphene introduces. In ref. [88], two types of graphene-based PCM devices are developed. One where graphene is patterned into nanoribbons and the other where the phase-change material (GST) is patterned into nanoribbons. Their device was found to need $<1\,\mu A$ SET and $<10\,\mu$ RESET currents. They also found that the off/on resistance ratios of their device was >100.

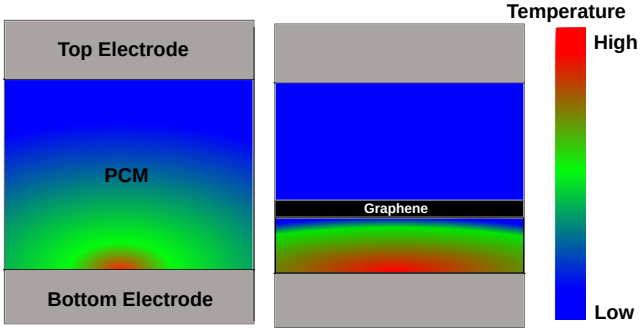

Figure 4. Illustration of phase change memory (PCM) devices with and without graphene. Note that the graphene-based device's lower PCM section contains a higher-temperature section with the same applied current.

3.8. Comparison of Graphene-Based Memristors with Different Switching Mechanics

Figure 5 and its accompanying **Table 1** compare the various aforementioned memristive properties based on the various switching mechanics discussed. To the best of the authors' knowledge, the values represented in both the table and figure are state of the art. As shown in all comparisons, graphene-based memristive devices have not fulfilled their maximum potential compared to their non-graphene counterparts. In some examples such as magnetic tunneling junctions (MTJs) and conductive filament, graphene-based memristive devices have improvements in switching energy. Graphene is often utilized as an electrode to lower energy consumption due to its higher out-of-plane resistance, so this result is not entirely unexpected.

Out of the aforementioned switching mechanics, PCM and conductive filament devices are by far the most widely studied for neuromorphic applications (particularly conductive filament devices.) Although Figure 5 suggests that PCM devices are weaker for neuromorphic applications, there are certain properties of these devices that make them more suitable. The retention plotted in Figure 5 is the maximum value at which the device have been tested. However, the device still held its retention at this point, and it is predicted that these devices can have retention on the order of 10 years.[67] Furthermore, the low HRS/LRS ratio is made up for by the fact that most PCM devices can be programmed in an analog fashion.[67] However, the most significant drawback of PCM devices is its large switching energy, even when graphene is introduced.

Graphene-based memristive devices have competitive advantages over non-graphene memristors, such as improvements in switching energy.[76] However, the ideal memristive candidate needs to have a wide variety of suitable properties. As shown in the radar plot in Figure 5, graphene-based memristive devices typically show lower endurance than non-graphene counterparts. This means that graphene-based memristive devices cannot perform as many operations, limiting their lifetime. For conductive filament devices, cycling endurance failures can be attributed to the aggregation of defects during cycling.[89,90] Hence, developing graphene-based memristive devices that limit the accumulation of defects is a logical step for neuromorphic investigations.

The switching mechanic most suited for further neuromorphic investigation is the conductive filament mechanism. As shown in Figure 5, the conductive filament device has a broad range of properties that are suitable compared to other switching mechanics that have limitations in certain areas. The graphene-based conductive filament device shows the highest potential for neuromorphic applications, if these devices can reach the same properties that non-graphene conductive filament devices have reached. While all of the aforementioned properties of memristive devices are important, some properties like switching energy, endurance, and retention should be prioritized over others, as they have more impact in neuromorphic architectures. Lastly, memristive devices (including conductive filament devices) still suffer from large variability.[91] Addressing this issue is challenging due to the stochastic physics underlying

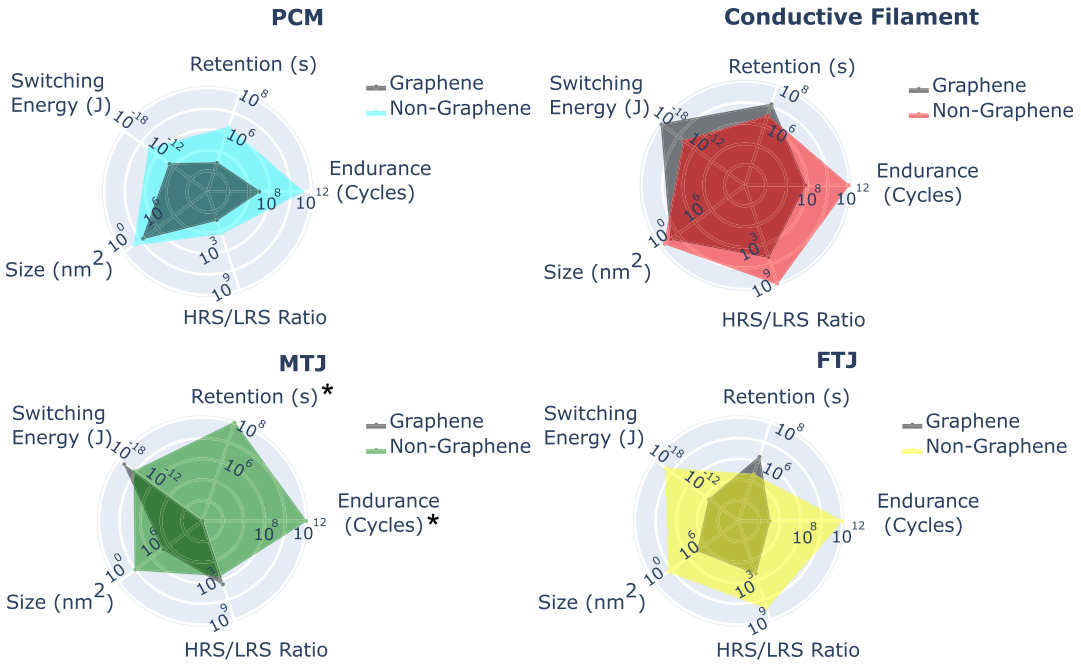

Figure 5. Radar plot comparing the various properties of memristors against different switching mechanics. The properties being plotted in the plot are displayed in Table 1. *Values for retention and endurance could not be found for graphene-based MTJs.

Table 1. Summary of key properties for graphene-based and non-graphene memristors and the sources which reported these values.

Resistive switching mechanic	Endurance		Retention		Switching energy		Size		R_{off}/R_{on} ratio	
Graphene-based memristors										
Graphene PCM	10^6 cycles	[87]	>300 s	[88]	1.5 nJ	[87]	2500 nm^2	[86]	≈10	[87]
Graphene CF	10^7 cycles	[77]	10^7 s	[164]	0.01 fJ	[27]	50 nm^2	[77]	≈10^6	[27]
Graphene MTJ	Not reported		Not reported		0.1 fJ	[165]	100 μm^2	[84]	10^5	[85]
Graphene FTJ	4000 cycles	[68]	3.45×10^5 s	[68]	50 nJ	[69]	50 μm^2	[69]	6000	[68]
Non-graphene memristors										
Non-graphene PCM	10^{11} Cycles	[166]	>3.6×10^5 s	[167]	≈0.3 pJ	[94]	78.53 nm^2	[168]	≈350	[169]
Non-graphene CF	>10^{12} cycles	[170]	>10^6 s	[171]	≈115 fJ	[172]	4 nm^2	[173]	10^9	[174]
Non-graphene MTJ	10^{12} cycles	[175]	3.15×10^8s	[176]	6 fJ	[177]	≈907.9nm^2	[178]	≈104	[179]
Non-graphene FTJ	10^8 cycles	[180]	10^4 s	[180]	≈1 fJ	[181]	314.1 nm^2	[182]	5.1×10^7	[183]

conductive filament devices; however, promising results have been achieved.[77,92] Strategies to close the gap between graphene and non-graphene memristive devices could include graphene structural/defect engineering,[93] reworking existing memristive device structures by adding graphene[94,95] and by proposing new device structures that aim to improve all relevant memristive properties, not just specific properties.

4. Graphene-Based Memristive Synapses

When developing SNNs, there are two fundamental building blocks: the neuron and the synapse. The synapse acts as a weighted connection between neurons. This weight is often referred to as the synaptic weight, and learning is introduced into neural networks by adjusting the synaptic weights following a certain mechanism.[96] Many unsupervised learning rules exist in neuromorphic architectures, such as the STDP,[97,98] SRDP,[99,100] paired pulse facilitation (PPF),[101] while there also exist supervised[102] and deep-learning-like[103] rules. **Figure 6** provides a visualization of some of the main neuromorphic learning rules implemented with memristors.

The most widely investigated rule in neuromorphic computing and memristive-based neuromorphic systems is, perhaps, the STDP rule. This is due to its biological plausibility as well as its relative simplicity. The STDP rule is where the individual timings of pre- and postsynaptic spikes dictate the synaptic weight update. Memristive implementations of the STDP rule require careful consideration of the action potentials presented to the device.[98,104]

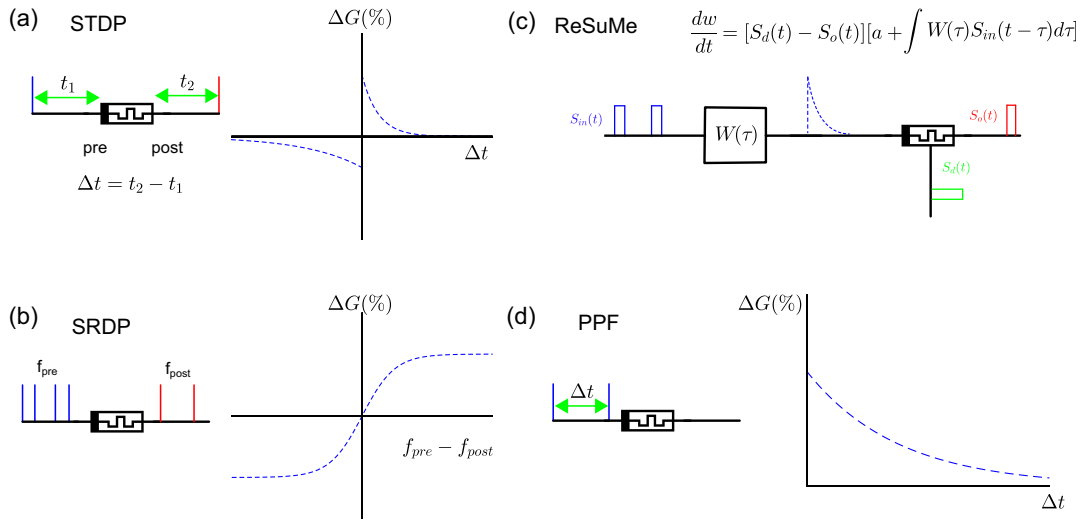

Figure 6. Summary of major neuromorphic learning rules demonstrated with memristors. a) Memristive demonstration of the general concept of the spike-timing-dependent plasticity (STDP) learning rule, where the timings of the pre- and postsynaptic spikes correlate to conductance change within the memristor. b) Demonstration of the memristive SRDP learning rule, where the difference in the firing rates of pre- and postsynaptic spike trains correlates to conductance change. c) Memristive demonstration of the ReSuMe learning rule. Note that the $W(\tau)$ refers to the window function used to convolute with the input and a is a biasing term. $S_d(t)$ acts as the supervisory signal and $S_{in}(t)$ and $S_o(t)$ refer to the input and output spike trains, respectively. d) Memristive demonstration of the paired pulse facilitation (PPF) learning rule.

Many graphene-based memristive devices have been characterized to behave as an artificial synapse, and these have been summarized in **Table 2**. In refs. [69,71], graphene-ferroelectric transistors were implemented as synapses. In ref. [69], an SL rule was used, known as the remote supervised method (ReSuMe).[102] In their work, they state that the ReSuMe method has many unique advantages compared to other SL methods used in SNNs, such as its capability of learning spike sequences as opposed to single spikes and that it is applicable to various types of neuron models. In ref. [70], graphene-based FETs were used as synapses capable of performing vector matrix multiplication. They also demonstrated their device's ability to allow for on-chip realizations of k-means clustering. However, the non-SNN synaptic devices are out of the scope of this paper and we will not investigate them in detail.

In ref. [27], a memristive device was developed by sandwiching aluminum, aluminum oxide, and graphene, where the graphene was used as the electrode. They characterized their device's STDP weight increase, i.e., potentiation, and decrease (depression) by applying 100 consecutive, positive/negative voltage pulses to it, and also demonstrated its ability to implement the STDP mechanism. Not only this, but the author of ref. [27] also demonstrated that their device exhibited metaplasticity, where the dynamics of the STDP rule change depending on the device's history.[78] is another work that demonstrates graphene's potential as a synapse capable of performing the STDP rule. In the device proposed in ref. [78], MoS_2 (another 2D material) was used as a switching medium and graphene as a bottom electrode.

Graphene oxide–based memristors are also researched for their neuromorphic applications. As already mentioned, unlike graphene, graphene oxide is hydrophilic, and is easily dispersible in organic solvents.[80] Works such as refs. [83,105–107] have all investigated graphene oxide–based synapses. In ref. [106], their device was capable of performing the STDP rule. By introducing gold nanoparticles to the device, an improvement in the R_{off}/R_{on} ratio was observed due to gold nanoparticles acting as charge-trapping centers. In ref. [107], a graphene-based crossbar array was used to hold synaptic weights as well as perform dot product operations. The device proposed in ref. [107] utilizes graphene oxide as the switching medium, as opposed to the electrode, due to graphene oxide's ability to contain oxygen vacancies. The STDP rule has also been implemented in ref. [83]. In this work, oxygen ions diffuse in the graphene oxide medium to form conductive filaments, and the device displayed reasonable endurance and retention properties. In ref. [105], a bilayer graphene-based device was also able to replicate the STDP rule while having modulatable plasticity, similar to ref. [27]. This modulatable plasticity was achieved through adjusting a back gate voltage being applied to the device.

Although STDP is very common for synaptic implementations, other learning rules are implemented as well. In some cases, no specific learning rule is tested for, but rather the device's ability to perform long-term potentiation (LTP) and short-term potentiation (STP). Investigations such as refs. [70,107,108] have investigated such instances, and these studies are often more focused on other aspects of the device. For example, in ref. [108], their work focuses more on the device's flexibility and ability to perform well after repeated stress.

Studies such as refs. [109-111] have emulated the SRDP rule; a rule which relates the spiking rates of pre- and postsynaptic neurons to modulate synaptic weight. In all three of these studies, graphene oxide was used, due to its ability to conduct protons. In ref. [112], a graphene oxide–based device was used to implement the PPF learning rule. This learning rule is a form of short-term plasticity where pairs of pulses, closely following each other, result in the second pulse having a higher excitatory postsynaptic current (EPSC). Authors of ref. [112] attribute their PPF behavior to residual protons in the indium zinc oxide (IZO) channel

Table 2. Summary of graphene and 12 sample non-graphene-based memristive synapses. Here, we have presented as many of the graphene-based neuromorphic synapses that could be found as well as 12 exemplar non-graphene-based memristive that represent each of the switching mechanics described in Section 3.

Paper	Device structure	Resistive switching mechanism	Size	Switching energy	Learning rule
Graphene-based					
[69]	Al/polyvinylidene fluoride (PVDF)/Cr–Au	Ferroelectric polarization	5 μm × 10 μm × 150 nm	50 nJ	ReSuMe[102]
[70]	Graphene/Al_2O_3/Pt/TiN/p++−Si	Interfacial polarization	0.5 μm × 1 μm × 120 nm	5 mJ	LTP/LTD
[27]	Al/AlO_x/graphene	Conductive filament (oxygen vacancy)	20 μm × 50 μm × 157 nm	0.01–1 fJ	STDP
[78]	Ni-Au/MoS_2/graphene/Ni–Au	Not investigated	24–36 μm^2	90 pJ	STDP
[83]	Ag/graphene oxide/FTO	Conductive filament (oxygen vacancy)	Not specified	9.6 μJ	STDP
[105]	Al/AlO_x/graphene	Conductive filament (oxygen vacancy)	9 μm × 360 nm	1 μJ	STDP
[106]	Al/graphene oxide–Au nanoparticle/ITO	Conductive filament (oxygen vacancy)	1 μm^2	150 nJ	STDP
[107]	Au/partially reduced graphene oxide/Au	Conductive filament (oxygen vacancy)	6 mm × 3 mm	11.2 mJ	LTP/LTD
[108]	Graphene/$WSe_{2-x}O_y$/graphene	Conductive filament (oxygen vacancy)	Not specified	16.1 pJ	STP/LTP
[109]	IZO/KH550-graphene oxide/ITO	Field effect transistor	80 μm × 1000 μm	66 μJ	SRDP
[110]	Ti–AU/chitosan-reduced graphene oxide/Ti–AU	Proton hopping	40 μm × 1 μm	8 nJ	SRDP
[111]	IZO/graphene oxide/ITO	Proton hopping	150 μm × 1000 μm	250 pJ	PPF and SRDP
[112]	Au/graphene oxide/ITO	Proton hopping	240 μm × 80 μm	12.5 μJ	PPF
[113]	Ta/Ta_2O_5/AlN/graphene	Conductive filament (oxygen vacancy)	Not specified	37 fJ	PPF
[55]	Ag/(nitrogen doped) graphene oxide quantum dots/Pt/Ti	Conductive filament (silver cation)	31 415 μm^2	900 μJ	PPF
[93]	TiN/AlN/graphene/Pd	Conductive filament (carbon filament)	31 415 μm^2	25 pJ	PPF/STDP
Non-graphene-based					
[184]	Ag/GeS_2/W	Conductive filament (Ag)	Not specified	15 pJ	Stochastic STDP
[185]	Ag/TiO_2/Pt	Conductive filament (Ag)	7853 μm^2	26 pJ	STDP/PPF
[186]	TiN/Hf/HfO_2/TiN	Conductive filament (oxygen vacancy)	100 nm^2	0.64 pJ	LTP/LTD
[187]	$Ge_2Sb_2Te_5$	Phase-change memory	1 μm × 10 μm	1 pJ	STDP
[188]	$Ge_2Sb_2Te_5$	Phase-change memory	39 nm technology	300 pJ	STDP
[189]	$Ge_2Sb_2Te_5$	Phase-change memory	70 685 nm^2	12.8 pJ	LTP/LTD
[190]	Ferromagnetic/MgO/ferromagnetic	Magnetic tunneling junction	3141 nm^2	38 fJ	Stochastic STDP
[191]	MgO/CoFeB/MgO/CoFeB	Magnetic tunneling junction	18 900 nm^2	1.2 pJ	STDP
[192]	Co/phenyldithiol/Co	Magnetic tunneling junction	3142 nm^2	5.6 μJ	Stochastic STDP
[193]	TiN/Si:HfO_2/SiON/Si	Ferroelectric polarization	500 nm × 500 nm × 28 nm	50 fJ	STDP
[194]	Pd/LSMO/$(BaTiO_{30.5}(CeO_2)_{0.5}$/STO/Si	Ferroelectric polarization	6362 μm^2	0.12 pJ	STDP/PPF
[195]	Pd/$BaTiO_3$–CeO_2/LSMO	Ferroelectric polarization	6362 μm^2	120 pJ	STDP

adding to the total proton concentration, resulting in a higher measured EPSC. Yan et al.[113] presented another work that has also demonstrated the PPF learning rule. Their study utilized a multilayer graphene electrode in a conductive filament memristive device to implement PPF, and achieved desirable spiking energy of 37 fJ. In ref. [55], an ECM-based device consisting of nitrogen-doped graphene oxide quantum dots, sandwiched between a platinum and silver electrode, was also used to perform the PPF learning rule. The use of graphene oxide quantum dots means that the device is biocompatible and biodegradable. Another study that investigated the PPF learning rule was ref. [93]. Interestingly, carbon plays a quite a significant role in the RS mechanic of the device, as the filament is formed by carbon. Furthermore, this synapse was also capable of performing the STDP rule as well.

To facilitate comparison with non-graphene-based memristive synapses, we also included, in Table 2, three representative devices from each of the switching mechanics we discussed in Section 3.4–3.7. Comparing memristive synapses is a difficult endeavor due to the many factors that need to be considered. In general, a graphene-based memristive synapse should operate with lower power consumption than its non-graphene counterpart with a similar device structure (if graphene is used as an electrode), due to graphene's higher out-of plane contact resistance.[76] However, other factors such as number of programmable states, variability, and switching time also play a critical role in the synaptic effectiveness of a memristive device. Furthermore, considerations should be made for any peripheral circuitry that is also required. For example, in some cases, selector or transistor circuits are required to limit the current flow through graphene-memristive

devices,[114,115] increasing the size and power consumption of the synaptic device.

5. Graphene-Based Memristive Neurons

As mentioned previously, the spiking neuron is an essential ingredient when designing SNNs. Generally, the neuron is designed such that a series of input voltage/current spikes increase what is known as the neuron's membrane potential, to a point where a threshold is reached. Once this membrane threshold is reached, the neuron produces an output voltage spike that propagates through the network. When designing neuronal circuits, many neuronal models exist ranging from the biologically accurate Hodgkin–Huxley model,[116] right through to the more computationally efficient and simple models such as the Izhikevich[117] and leaky integrate and fire (LIF)[118] models. The fundamental trade-off of biological plausibility and computational simplicity often leans in favor of computational simplicity when designing neuromorphic circuits, with the LIF model being the most common choice.

Although it is more common to use memristors as synapses, there have also been investigations dedicated to implementing memristive devices into neuronal circuits. Utilizing the unique characteristics of memristors when designing these circuits can result in reduced size and power consumption, while also retaining the fundamental properties of neurons. Although many memristive neuron designs exist in the literature, only a few of them are using graphene-based memristors. These designs have been summarized in **Table 3**. For this table, all major memristive neuron designs found in the literature were considered (graphene and non-graphene), and their key attributes such as components used, neuron model, energy consumption, etc., have been summarized.

In ref. [119], two memristive LIF neuron models are proposed. The first one is the most minimal design, consisting of a constant voltage source, a volatile memristive device, and a capacitor. This first model (referred to as MIF or MIF1) is able to replicate two key voltage levels in spiking neurons: the resting potential and the neuron threshold voltage. The second design, i.e., MIF2, adds an additional volatile memristor and a constant voltage source to MIF1. With this change, the design is able to replicate a third voltage level found in spiking neurons, the reset potential. The authors of ref. [119] experimentally validated their neuron design using off-the-shelf components and found that, when connected to a solid-state brain network, their neurons had a similar power consumption to the human brain, which equated to approximately 12.8 pJ neuron^{-1}. Due to the ideal parameters of this design such as minimal components, low spiking energy, and desirable operating range, this work is considered to be one of the leading works in memristive neuron design.

In ref. [120], a memristive emulator was used to develop a unique neuron model. In their design, biologically accurate action potentials were presented to their neuron, and by controlling a fixed internal voltage source, they were able to replicate many different spiking behaviors that are akin to those found in biological neurons. Kim et al. (ref. [121]) also reported fabricating a Ag/HfO$_x$:N/Ag memristive device to develop an LIF neuron. In this work, various characteristics of biological neurons are retained, such as all-or-nothing spiking, the refractory period, strength-modulated frequency, and threshold-driven spiking. In ref. [122], a quasi-LIF neuron was developed where the membrane timing constant τ was not held constant, but rather, modified based on the principle of homeostatic plasticity.

Table 3. Summary of non-graphene- and graphene-based memristive neuron designs.

Paper	Neuron model	Energy usage	Components used[a)]	Output voltage /current	Threshold voltage
Non-graphene-based					
[119] (MIF1)	LIF	4.9 pJ Spike^{-1}	1 M + 1 C + 1 VS	−70 to −50 mV	−48 mV
[119] (MIF2)	LIF	12.8 pJ Spike^{-1}	2 M + 2 VS + 1 C	−80 to −50 mV	−52 mV
[120]	Spiking and bursting	60–110 nJ Spike^{-1}	1 M + 3 T + 2 VS + 1 C	0–2 V	N/A
[121]	LIF	4 nJ Spike^{-1}	1 M + 1 C + 1 R	0–1 V	0.19 V
[124]	LIF	4 μJ Spike^{-1}[b)]	1 M + 1 C + 2 R	0–2 V	1 V
[125]	LIF	5.6 fJ Spike^{-1}	2 M + 2 VS + 2 C + 2 R	−2–2 V	Not specified
[126]	LIF	17.7 nJ Spike^{-1}	1 M + 1 C + 2 R	0–0.4 V	0.7 V
[127]	LIF	23μJ Spike^{-1}	1 M + 1C + 1 R	0–1 V	0.5 V
[128]	LIF	660 pJ Spike^{-1}	2 M + 1C + 1 R + 1VS	0–0.4 V	Not specified
[129]	LIF	0.3 nJ Spike^{-1}	1 M	10^{-9}–10^{-4} A	4 V
[130]	LIF	25nJ Spike^{-1}	1 M + 1C + 1 R	0–25 μA	–
Graphene-based					
[58]	LIF	20 pJ Spike^{-1}[b)]	1 M + 1 C + 3 R	0–1 V	4 V
[112]	LIF	10 pJ Spike^{-1}[b)]	1 T	100 nA	0.5 V
[131]	LIF	500 pJ Spike^{-1}	1 M + 1 C + 3 R	90 nA	Not specified

[a)] M = memristor; C = capacitor; R = resistor; VS = voltage source; T = transistor. [b)] These values were calculated by E = voltage × current × spike duration.

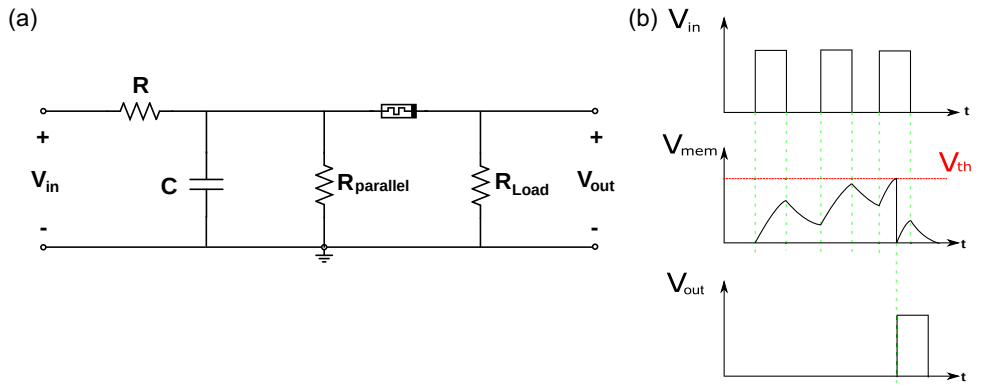

Figure 7. a) Memristive neuron circuit capable of replicating the spiking behaviors of the LIF neuron; b) illustration on how the applied input voltages generate an output spike.

Homeostatic plasticity is a phenomenon that constrains a neuron's firing rate to a semifixed rate, and has been utilized in neuromorphic networks to enhance the results.[123] Throughout the investigations in the literature, no memristive designs have implemented such a mechanism, owing to the increased complexity of doing so. This is one avenue of memristive neuron design that could potentially be explored.

Neuron designs such as[121,124–130] volatile memristors are used to develop LIF neuron circuits, similar to the circuit in **Figure 7**a. When input spikes are presented to this circuit, the capacitor begins to charge the circuit, reflecting the increase in the neuron's membrane potential. The threshold is dictated by the memristor's threshold switching mechanism, so once the membrane potential is sufficient, the device switches to a low conductance state. This produces an increase in current toward the load side, thus producing an output spike.

Graphene-based memristive neuron designs such as those proposed in refs. [58,112,131] have also been investigated. Wan et al.[112] utilized graphene oxide in a neuron transistor, which was also capable of performing synaptic functions. Interestingly, in this work, their device was implemented into an orientation detection task, where the orientation of a grating pattern is determined in a neuromorphic manner. The results of this experiment showed comparable results to biological visual systems. However, their neuron design only demonstrated the dendritic integration aspect of most designs and did not demonstrate postsynaptic events. In refs. [58,131], both graphene and another 2D material (MoS_2) were used in the memristive device, and their artificial neuron was capable of replicating key behaviors of biological neurons, such as post-firing refractory period and strength-modulated frequency response. In ref. [58], the design of ref. [131] was improved upon by using a vertically structured device. This effect is attributed to the fact that the RS mechanism in these devices is mediated by the grain boundaries in MoS_2; hence, the vertically oriented device can be scaled.

6. Graphene Memristive Neuromorphic Networks

Some studies have taken their investigations to the next step by using graphene-based memristors in traditional neural networks and spiking neuromorphic architectures. Works such as refs. [106,107] have investigated their device's performance in traditional artificial neural networks.[107] It is demonstrated that their network could classify various flowers when information such as the sepal length, sepal width, petal length, and petal width was presented. When they implemented their device as a synapse, a classification accuracy of 93.3% was achieved compared to 96.7% that was achieved through ideally mapped conductance values. In ref. [106], the graphene-based device's ability to replicate an input image was tested in a neuromorphic network. This was done by using the STDP rule, and after 30 iterations the image was successfully replicated.

There exist few, well-established benchmarks that are used to compare performances across different neuromorphic networks.[132] This is largely owing to the difficult nature of developing learning algorithms capable of processing voltage/current spikes.[132] One benchmarking test that is used in neuromorphic circles is the classification of the Modified National Institute of Standards and Technology (MNIST) dataset, using a network similar to the one demonstrated in **Figure 8**. The MNIST dataset is a series of 28×28 gray scale images representing handwritten numeric characters (0–9). To train and test SNNs similar to the one shown in Figure 8, to perform MNIST classification, it needs to encode the input images into voltage/current spikes. One of the most common methods for this is to encode each pixel into Poissonian voltage/current spike trains where the average spiking frequency is proportional to the pixel intensity. Another similar method is to binarize the MNIST image and then encode the binarized image with Poissonian spike trains with two different spiking frequencies. Although this method reduces the information contained within the image, the encoding circuitry required is significantly simplified. To our knowledge, except for simulation attempts to use graphene-based memristive devices in a neuromorphic architecture,[133] no previous work has attempted MNIST classification using graphene-based memristive synapses, thus it is difficult to assess how effective these devices are compared to other devices.

Other SNNs have been developed to perform other tasks with graphene-based devices. In ref. [69] an SNN was used to classify 3×3 binary images, specifically the characters "z," "v," and "n." Their network utilized a graphene-based ferroelectric transistor designed to perform SL, specifically the ReSuMe SL.[102]

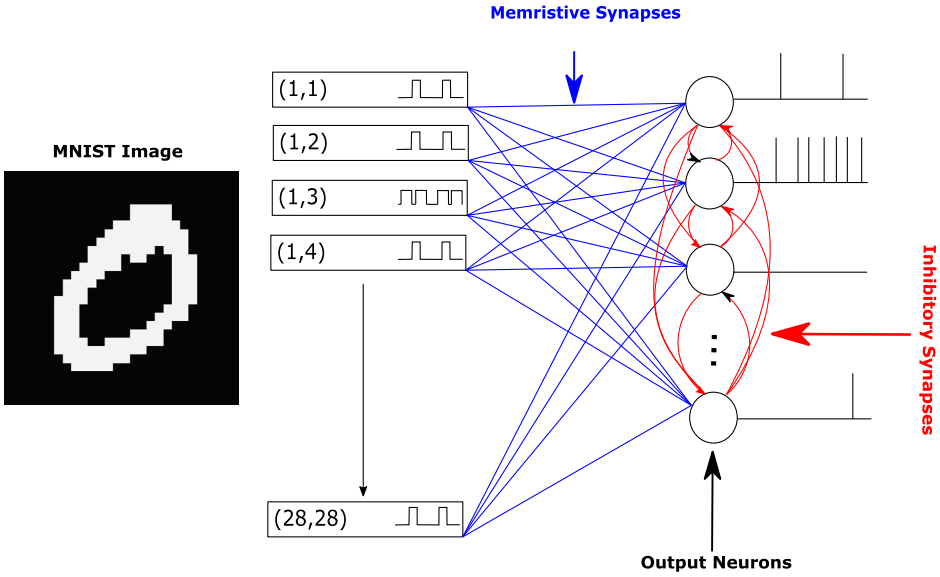

Figure 8. A simple spiking neural network (SNN) architecture that can be used to perform unsupervised MNIST learning and classification. The output neurons, which are fully connected to all the input image pixels' spiking trains through learning synapses, are also connected using inhibitory synapses that introduce learning competition. Adapted with permission.[133] Copyright 2022, Authorea.

In ref. [134], graphene nanoribbons were structured to form a synapse capable of implementing the STDP rule. These nanoribbons were then implemented into SNNs in works such as refs. [135–137]. In all three of these works, classification of five alphabetic characters in a 5×5 binary image was performed.

SNNs are often touted for their abilities to perform specific tasks in a more efficient manner compared to traditional deep-learning networks. These tasks are often attributed to event-driven data (such as data from a dynamic vision sensor), given that one of the main advantages of neuromorphic networks is that they are event driven. As such, testing graphene-based devices in networks performing tasks well suited for neuromorphic platforms is another critical area of research.[138,139] In ref. [138], two graphene excitable lasers were connected in cascade to perform a simple coincidence detection task. In this work, the optical properties of graphene are utilized to create an optoelectronic laser capable of spike processing, akin to an LIF neuron. The neuromorphic task of performing coincidence detection of two photons is significant for spatiotemporal pattern recognition. In ref. [139], graphene–insulator–graphene memristive devices were implemented as synapses to perform 2D motion detection. A physics-based, SPICE-compatible model was used to emulate the synaptic device, which had previously been characterized in ref. [140].

Comparison of graphene and non-graphene memristive devices implemented into SNNs is a difficult endeavor. As mentioned previously, few works have developed graphene-based SNNs that are comparable to previous works that have attempted the same task. However, for typical graphene-based memristive devices, one expectation is that the overall energy efficiency of the network is increased, due to graphene's lower power consumption. However, other factors such as network output/accuracy, size, etc., are dependent on design choices like the learning rule used, the network topology, the neuron model chosen, etc. Thus, the choice of which memristive device is dependent on these design choices. Another element that is often not explored is the versatility of graphene-based memristive devices. The memristive structures proposed for graphene-based memristive devices are often based on the synaptic function that they emulate. For example, the graphene-based memristors used to perform rules like STDP[27,83] operate very differently to the graphene-based memristors that implement the PPF learning rule,[111,112] where the latter often uses proton conduction for this effect. Compared to works like ref. [141], which have demonstrated synapses capable of performing multiple functions, it may be ideal to investigate multipurpose graphene-based memristive synapses.

7. Discussion and Prospects

Graphene has often been implemented in photonics as well as electronics applications. However, other than neuronal and synaptic applications, graphene has also found other use cases in neuromorphic computing. For example, Shastri et al.[138] coupled graphene with a laser system to demonstrate low-level spike processing. In their work, graphene was used as a saturable absorber, due to its high saturable absorption-to-volume ratio. They also demonstrated their system's capability to perform coincidence detection. Another neuromorphic application of graphene is used in triboelectric nanogenerators. Triboelectric nanogenerators can serve as energy conversion or can serve as sensors in self-powered neuromorphic systems, and graphene has been used in conjunction with these designs in various works.[142–145] Furthermore, graphene has also been implemented in non-memristive devices for both synaptic and neuronal applications. Studies such as refs. [134,146] have utilized patterned graphene nanoribbons to illustrate synaptic and neuronal applications, respectively.

Many issues still exist in the field of developing graphene-based memristive devices for neuromorphic computing architectures. Broadly speaking, these problems can be classified into two categories: device-level and network-level problems, which will be discussed in this section.

7.1. Device Level Issues

Many graphene-based and non-graphene-based devices have been developed for neuromorphic purposes. However, these developments usually are impacted by some device-level constraints and challenges. Issues such as DTD and CTC variability still plague device fabrication today.[147] Although the stochasticity in DTD and CTC variations of fabricated memristors limits the ability to control the device's conductance (and other properties), it can be exploited in neuromorphic settings to overcome other issues, such as "overfitting." Overfitting happens when a network fails to generalize because it is tuned mainly to the training data.[148] By utilizing this stochastic property, previous research has shown that overfitting problem can be overcome.[149]

Some research efforts have been dedicated to eliminating variability by tuning the device fabrication process. For example, in ref. [150], Winkler et al. found that the orientation of the crystal structure in HfO_2 played a significant role in the forming voltage and the memristor's variability. They suggest that the grain boundaries within the HfO_2 control the energy and orientation required to form conductive filaments, and thus proposed controlling the grain boundaries in memristive devices for improved performance. In ref. [151], it was noted that the removal of SrO in their Ti-terminated $SrTiO_3$-Pt devices reduced the memristive device's variability at the expense of reduced retention. Graphene memristors have also been engineered to reduce variability, in works like ref. [152], where filament formation due to reduced graphene oxide can be controlled by modulating the ambient temperature and humidity.

The issue of variability is also being addressed at the network level, where works such as refs. [123,153,154] implement algorithms that account for the memristor's inherent variability. For example, in ref. [123], a network was designed with a simplified STDP learning rule. This simplified rule meant that device non-idealities had less effect on the network's output. In ref. [153], a twin-memristive synapse (where two memristors instead of one are used) showed little degradation in the final results until the simulated dispersion of the memristive parameters was increased to 15%.[154] also used a multi-memristive approach to mitigate device variability, where each synapse consisted of two memristors responsible for excitatory and inhibitory connections.

Furthermore, due to graphene's high conductivity, graphene-based memristive devices suffer from a larger current draw, particularly in their LRS. This problem can be solved by current limiter circuits,[155,156] which limit the maximum amount of current presented to the device. In its simplest form, a current limiter can be a transistor connected in series with the memristive device.[156] Other works such as ref. [155] use other simple components like load resistors to limit the current. Although these methods lower the current, the added circuitry increases the difficulty in manufacturing.

Fabricating graphene in large volumes and in a sustainable manner is another issue facing graphene-based memristive devices. The CVD and PECVD methods are often touted as being the dominant method for producing graphene in large volumes, and works such as refs. [17,45-47,157] have demonstrated the sustainable fabrication of graphene using them. However, fabricating graphene-based memristive devices in large volumes still proves to be a challenge. This is due to the difficult nature of generating uniform, defect-free graphene on a large scale. Another area of interest in graphene fabrication is to further simplify the PECVD through the use of atmospheric pressure microwave plasma.[158] In this work, the plasma is produced under atmospheric conditions, removing the need to create vacuums and heating. Importantly, this reduces the cost and complexity of graphene production.

7.2. Network-Level Issues

Network-level issues are those that relate to the neuromorphic architectures in which the graphene-based devices are implemented. One of the biggest issues is creating arrays known as crossbars to connect multiple neurons with synapses. A crossbar array is one of the most common architectures for efficient and flexible connections among neurons. Unfortunately, large-scale crossbar architectures suffer from many issues, including increased word and bit line resistance with increased size, increased delays, and large current draw.[8] Solutions do exist in the forms of adding peripheral circuitry to these crossbar arrays but unfortunately, these circuits often consume the most amount of power (≈57%).[159]

Crossbars also suffer from issues such as sneak paths. Sneak paths form when several memristors in low conductance states can provide alternate paths within the crossbar to the selected memristive device and thus alter its conductance. This problem is unique in that it can be dependent on the values stored within the memristive device. Potential solutions to the sneak path issues exist. One solution is to use a complementary RS scheme, where pairs of memristors in opposite states are used.[160] Alternatively, it is also possible to perform read and reset operations in parallel while using set-only selected cells to also overcome this problem.[161] Another solution is to build active crossbars using components such as transistors, diodes and selectors.[162]

Another network-level issue is a lack of existing benchmarks for neuromorphic computing. Although many benchmarks such as the MNIST dataset exist for deep learning, they are not as widely used in neuromorphic benchmarking, especially when it comes to more advanced devices such as graphene-based neurons and synapses used in unsupervised learning.[133] Instead, tasks that favor neuromorphic systems, such as classifying data from event-based vision sensors,[163] are preferred, due to their inherent event-based nature. Few of these neuromorphic datasets exist, which has resulted in a lack of comparisons between neuromorphic networks, making it difficult to assess and improve upon existing networks.

7.3. Future of Graphene-Based Memristors

The upside to using graphene-based memristors in neuromorphic computing is enormous. Memristive devices generally

suffer from high degrees of CTC and DTD variation. However, graphene-based memristors can potentially overcome this flaw. As noted in Section 3.5, defect engineering in graphene can result in more concentrated filament formation and thus reduce this variability. Furthermore, the manufacturing techniques outlined in ref. [152] show that controlling the ambient conditions in which the memristive device is fabricated can potentially improve its reliability. Another key upside is the potential for extremely low power electronics. In ref. [27], a memristive device with below femtojoule switching requirements was achieved, further adding to the low power ideals of neuromorphic computing. Another upside is the potential green fabrication of memristive devices,[17] paving the way for low-cost and sustainable manufacturing practices.

8. Conclusion

Graphene-based devices can bring significant benefits to neuromorphic computing and improve neuromorphic architecture applications, due to the superior electrical, mechanical, and thermal properties they offer. In this article, we discussed how graphene-based memristive devices can be used to develop neuromorphic synapses and neurons. We showed that, due to its high conductivity, graphene is often utilized as an electrode in neuromorphic neurons and synapses, but it can also be used in other neuromorphic settings.

We conclude that there is still a gap between graphene- and non-graphene-based memristive designs, in terms of their important neuromorphically relevant characteristics such as size, switching energy, endurance, retention, and R_{off}/R_{on} ratio. This gap needs to be addressed by the research community before we can bring graphene's benefits to neuromorphic architectures and implement graphene-based neural networks that combine both graphene-based synapses and neurons in a niche study area, which needs significant future investigations.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

graphene, memristors, neuromorphic, neurons, spiking neural networks, synapses

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