

## Article

# A Novel Floating High-Voltage Level Shifter with Pre-Storage Technique

Qiang Li <sup>1,2</sup> , Yuan Yang <sup>1,\*</sup>, Haohao Ma <sup>1</sup>, Yangle Zhou <sup>1</sup>, Guolong You <sup>1</sup>, Minmin Zhang <sup>1</sup> and Wei Xiang <sup>3,4</sup> 

<sup>1</sup> Department of Automation and Information Engineering, Xi'an University of Technology, Xi'an 710048, China; lq@bttc.edu.cn (Q.L.); mahaohao@stu.xaut.edu.cn (H.M.); yanglezhou@stu.xaut.edu.cn (Y.Z.); youguolong@stu.xaut.edu.cn (G.Y.); minminzhang@stu.xaut.edu.cn (M.Z.)

<sup>2</sup> School of Physical Science and Technology, Baotou Teachers' College, Baotou 014030, China

<sup>3</sup> School of Engineering and Mathematical Sciences, La Trobe University, Melbourne, VIC 3086, Australia; w.xiang@latrobe.edu.au

<sup>4</sup> College of Science and Engineering, James Cook University, Cairns, QLD 4878, Australia

\* Correspondence: yangyuan@xaut.edu.cn

**Abstract:** This paper proposes a novel floating high-voltage level shifter (FHV-LS) with the pre-storage technique for high speed and low deviation in propagation delay. With this technology, the transmission paths from input to output are optimized, and thus the propagation delay of the proposed FHV-LS is reduced to as low as the sub-nanosecond scale. To further reduce the propagation delay, a pull-up network with regulated strength is introduced to reduce the fall time, which is a crucial part of the propagation delay. In addition, a pseudosymmetrical input pair is used to improve the symmetry of FHV-LS structurally to balance between the rising and falling propagation delays. Moreover, a start-up circuit is developed to initialize the output state of FHV-LS during the  $V_{DDH}$  power up. The proposed FHV-LS is implemented using 0.3- $\mu\text{m}$  HVCMOS technology. Post-layout simulation shows that the propagation delays and energy per transition of the proposed FHV-LS are 384 ps and 77.7 pJ @  $V_H = 5$  V, respectively. Finally, the 500-points Monte Carlo are performed to verify the performance and the stability.

**Keywords:** floating high-voltage level shifter; low propagation delay; pre-storage; regulated strength; pseudosymmetry; HVCMOS



**Citation:** Li, Q.; Yang, Y.; Ma, H.; Zhou, Y.; You, G.; Zhang, M.; Xiang, W. A Novel Floating High-Voltage Level Shifter with Pre-Storage Technique. *Sensors* **2022**, *22*, 1774. <https://doi.org/10.3390/s22051774>

Academic Editors: Zahir M. Hussain and Giuseppe Ferri

Received: 3 January 2022

Accepted: 22 February 2022

Published: 24 February 2022

**Publisher's Note:** MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.



**Copyright:** © 2022 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

## 1. Introduction

With the increase in power density and switching speed of the power devices, gate drivers with low propagation delays and high operating frequencies are in high demand [1–3]. In the application of feedback-based regulation, the gate drivers are developed to operate in the closed-loop mode to respond to the change of loads [4–6]. Moreover, some gate drivers feature functions of over-current protection and fault indication [7,8]. For precise regulation and fast protection, low propagation delay is critical for gate drivers. In commercial applications, the propagation delay of state-of-the-art gate drivers is in the order of ten nanoseconds, excluding the delay induced by bonding wires and pads. In gate drivers, multi-voltage power supply technology is applied to balance between switching speed and power consumption [9,10]. The digital units implementing the logic processing are supplied by low voltage to reduce power dissipation, while the circuits composing the output stage are powered by high voltage to carry enough energy for loads. For communication between circuits supplied with different voltage, the level shifter becomes a critical interface in the gate driver [11,12]. In the medium/high-voltage gate driver or half-bridge gate driver, FHV-LS can transfer the control signal from low-side power rail to high-side power rail with floating-ground, sending commands to the output of gate driver. For the high-speed gate driver, the FHV-LS with nanoseconds of propagation delay will have a negative impact

on the total propagation delay in gate driver. Therefore, the reduction in propagation delay of FHV-LS will be an essential destination for high-speed gate driver design.

On the one hand, the existing level-shifting circuits have large propagation delays, which are not suitable for high-speed applications. Especially in feedback-based regulation and protection situations, large propagation delay not only affects the regulating accuracy but also suffers from the risk of damage. On the other hand, large propagation delay will lead to major deviation between rising and falling propagation delay. As the operating frequencies increase, the distortions in duty cycle caused by the deviation become more serious. Therefore, this study focuses on the analysis of factors affecting the propagation delay and methods to reduce the propagation delay and the deviation of FHV-LS. The main contributions of our work are outlined as follows:

- A novel level-shifting circuit structure with pre-storage technology is proposed to achieve low propagation delay. Then, the design approach and implementation of the proposed FHV-LS are presented.
- Based on the proposed FHV\_LS, the propagation delay is analyzed in detail. Moreover, the factors affecting the propagation delay are revealed for an in-depth insight into the proposed FHV-LS.
- To further improve the performance of the proposed FHV-LS, the pull-up network with regulated strength technology and the pseudosymmetrical input structure are introduced to optimize the propagation delay and the deviation of the proposed FHV-LS, respectively. In addition, a start-up circuit applied to the register is developed to initialize the output state of FHV-LS during  $V_{DDH}$  power-up. With the start-up circuit, the output of FHV-LS always follows the input correctly in any operating condition.

The remainder of this paper is organized as follows. Section 2 reviews the conventional FHV-LSs, and three topologies are summarized. Section 3 presents the design principle and implementation of the proposed FHV-LS and also analyzes the propagation delay. Section 4 proposes three improvements to optimize the propagation delay, deviation, and start-up. The performance of post-simulation is shown in Section 5. Section 6 concludes our work.

## 2. Review of Conventional FHV-LSs

Many FHV-LSs have been proposed in the literature [13–29] to reduce the propagation delay. According to the structures, three topologies (Topology-I, Topology-II, and Topology-III) are summarized in Figure 1. The devices in orange dashed boxes are placed in HV-NWell (HVNW). The body of HVNW biased with  $V_{SSH}$  can tolerate high voltage. Consequently, the devices in HVNW could operate in the floating high-voltage domain between  $V_{DDH}$  and  $V_{SSH}$ . The devices in blue dashed boxes are HVMOS whose drain source and drain gate can handle high voltages, but its gate source switches in the low voltage range.

### (1) Topology-I: DC-LS

The first topology of FHV-LS is direct-coupled level shifter (DC-LS), as depicted in Figure 1a. The HV-NMOS transistors  $N_{1H}/N_{2H}$  are used to convert the input signal  $V_{INL}$  into its drain current. The HV-PMOS transistors  $P_{1H}/P_{2H}$  transfer its drain current into voltage and isolate the high drain voltage to protect the devices in HVNW. The NMOS  $N_1/N_2$  are used to clamp the voltage  $V_A/V_B$  to not fall below  $V_{SSH}$ . The DC-LS in [13,14] is a basic structure of FHV-LSs which features a simple structure and fewer components. The circuits are fabricated using silicon-on-insulator (SOI) technology to improve the voltage rate, but it has a large propagation delay and poor symmetry between the rising and falling propagation delays. The asymmetry between rising and falling propagation delay will induce deviation, which will increase with the decrease of propagation delay. To reduce the static power consumption, the input of FHV-LS is activated by a short pulse generator [15,16], but the propagation delays are still unsatisfactory, and the deviation between rising and falling propagation delay in [15] is not optimized. The DC-LSs proposed in [17,18] decrease the propagation delay and optimize the symmetry between the rising

and falling propagation delays; however, the propagation delay is at least 2 ns. The nanosecond delay may not meet the needs of high-speed applications.

### (2) Topology-II: CM-LS

The second topology of FHV-LS structure is the current-mirror level shifter (CM-LS), as shown in Figure 1b. Compared with DC-LS, CM-LS has a large quiescent current induced by the current mirror. To improve the power efficiency, the HVNMOS transistors  $N_{1H}/N_{2H}$  of CM-LS are controlled by pulse signals. Reg is a register to hold the output state. The current mirrors, composed of  $P_1/P_2$  and  $P_3/P_4$ , are used to change the state of Reg according to the input state of  $V_{INL}$ . The diodes  $D_1/D_2$  are reversely paralleled with  $P_1/P_3$  to clamp the voltage  $V_A/V_B$  to protect the devices in HVNW. The CM-LS in [19–21] utilizes a short pulse generator to control HV-MOS  $N_{1H}/N_{2H}$ . With signal conversion, the state of the latch unit is changed by the short pulse current. To reduce power consumption, an instantaneous-power-consuming level shifter is proposed to increase the efficiency [22] since the output detector is used to turn the level shifter off before the delay time. The CM-LSs proposed in [23–25] alter the state of RS-trigger by the voltage cross a resistor. This structure is commonly found in higher-voltage level shifters. It also needs the Schottky diodes in reverse parallel across the resistors to protect the devices in HVNW. Considering the influence of the process, temperature, and parasitic effect, the pulse width of the short pulse should have enough margins to guarantee that the latch unit can be flipped reliably. However, extending the width of the input pulse will lead to an increase in the power consumption and design complexity. Therefore, the pulse width should be optimized according to the power consumption and performance.

### (3) Topology-III: CC-LS

The third topology of FHV-LS is a capacitor-coupled level shifter (CC-LS), as shown in Figure 1c. High-voltage capacitors,  $C_1$  and  $C_2$ , are used to shift the input signal  $V_{INL}$  to the output  $V_{OH}$  with the high common-mode voltage. The CC-LS proposed in [26] has a propagation delay of 0.5 ns and low static current consumption, but requires an off-chip capacitor to enhance the power PMOS driving capability. The CC-LS in [27] integrates two on-chip capacitors (both 60 fF) to shift the signal from  $V_{INL}$  to  $V_{OH}$ , but the rising/falling propagation delay of 1.45 ns/1.3 ns is large for the 180 nm process. The CC-LS in [28] achieves a 0.5 ns propagation delay with two 2 pF on-chip capacitors. The CC-LS in [29] achieves a 115 ps propagation delay by isolated low-voltage NMOS transistors and capacitive coupling, but the current mirror of the level shifter in [28,29] is not turned off after converting, resulting in high power consumption.

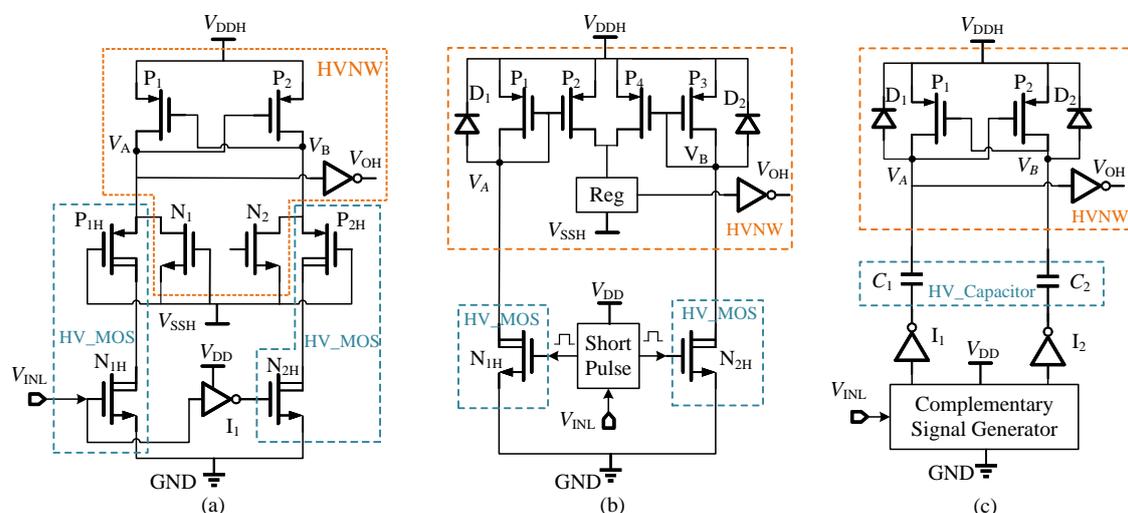


Figure 1. Three topologies of FHV-LS: (a) DC-LS, (b) CM-LS, (c) CC-LS.

### 3. Proposed FHV-LS

#### 3.1. Design Approach of Proposed FHV-LS

The gate drivers with FHV-LS are commonly used to control the power devices. However, the electrical noise generated by power circuits is also coupled to the driver stage by means of electricity or magnetism. To reduce the risk of false trigger, optocouplers are applied to achieve electrical isolation between the control signals and the high-voltage signals. Then, the optocoupler transmits the control signal to the input of the level-shifting circuit as shown in Figure 2. The proposed FHV\_LS is composed of high-side circuit and low-side circuit. The high-side circuit consists of C/V converter, registers (pre-Reg, read-Reg), and CLK generator. The V/C converter on the low side converts the input voltage into the current signal  $I$ . The C/V converter on the high side then transforms the current  $I$  into the voltage  $V$  which is the input to the CLK generator and pre-Reg. The CLK generator generates the control signals  $V_{CK1}$  and  $V_{CK2}$  to enable the pre-Reg and read-Reg in the latch or transfer mode. If pre-Reg operates in the transfer mode, the output of the C/V converter is stored in pre-Reg, while read-Reg works in the latch mode to hold  $V_{OH}$ . Conversely, pre-Reg operates in latch mode, and read-Reg is in transfer mode to transmit the output of pre-Reg to  $V_{OH}$ . Based on the mode switching for registers, the “next” state of  $V_{INL}$  is loaded in pre-Reg in the steady state. During the switching of  $V_{INL}$ , the input state restored in pre-Reg is transmitted to the output  $V_{OH}$  under the control of  $V_{CK1}/V_{CK2}$ . In other words, the present state of  $V_{INL}$  is transmitted to  $V_{OH}$ . Therefore, the propagation delay of FHV-LS is determined by the delay from  $V_{INL}$  to  $V_{CK2}$ .

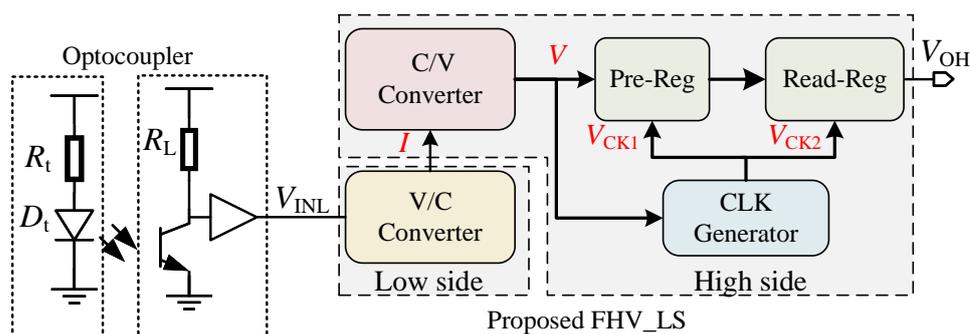


Figure 2. Topology of the proposed FHV-LS.

#### 3.2. Implementation of the Proposed FHV-LS

The implementation of the proposed FHV-LS is depicted in Figure 3. It involves two power rails, namely the low-side power rail ( $V_{DD}-GND$ ) and the high-side power rail ( $V_{DDH}-V_{SSH}$ ). The V/C converter on the low side is composed of HV-NMOS ( $N_{1H}-N_{2H}$ ) and inverter  $I_1$ . The logic states of  $N_{1H}$  and  $N_{2H}$  are flipped by  $I_1$ . The C/V converter on the high side consists of transistors ( $P_1-P_2, N_1-N_2$ ), inverters  $I_{A1}-I_{A2}, I_{B1}-I_{B2}$ , and HV-PMOS ( $P_{1H}-P_{2H}$ ). The CLK generator is composed of the Nand gate  $A_1$  and inverter  $I_2$ . The pre-Reg/read-Reg registers controlled by  $V_{CK1}/V_{CK2}$  are clock-controlled RS flip-flops. The signal transmission paths of proposed FHV-LS from  $V_{INL}$  to  $V_{OH}$  are highlighted with red and blue dashed lines during  $V_{INL}$  witches. To make the formula clear, “0/1” represent logic low/high for the high-side and low-side logic signals.

The operating process of the proposed FHV\_LS is depicted as shown in Figure 4. We assume that  $V_{INL} = 0$  is the initial input state. In this state,  $N_{1H}, N_1, P_{2H}$ , and  $P_2$  are turned off.  $N_{2H}, N_2, P_{1H}$ , and  $P_1$  are turned on and operate in the linear region. So,  $V_A = V_{A2} = V_{B1} = 1, V_{A1} = V_B = V_{B2} = 0$ . The outputs of the CLK generator are  $V_{CK1} = 0$  and  $V_{CK2} = 1$ . According to the register, pre-Reg operates in the transfer mode, while read-Reg is in the latch mode. The output of pre-Reg is determined by the logic of  $V_{A1}$  and  $V_{B1}$ , so  $Q_1 = 1$ . It indicates that the next state of  $V_{INL}$  is loaded in pre-Reg in the steady state. For the latch mode of read-Reg, it is worth mentioning that the output of read-Reg is

an uncertain value during  $V_{DDH}$  power-up. So, the start-up circuit is required to force the output state of read-Reg to be  $V_{OH} = 0$ . The start-up circuits will be discussed in Section 4.

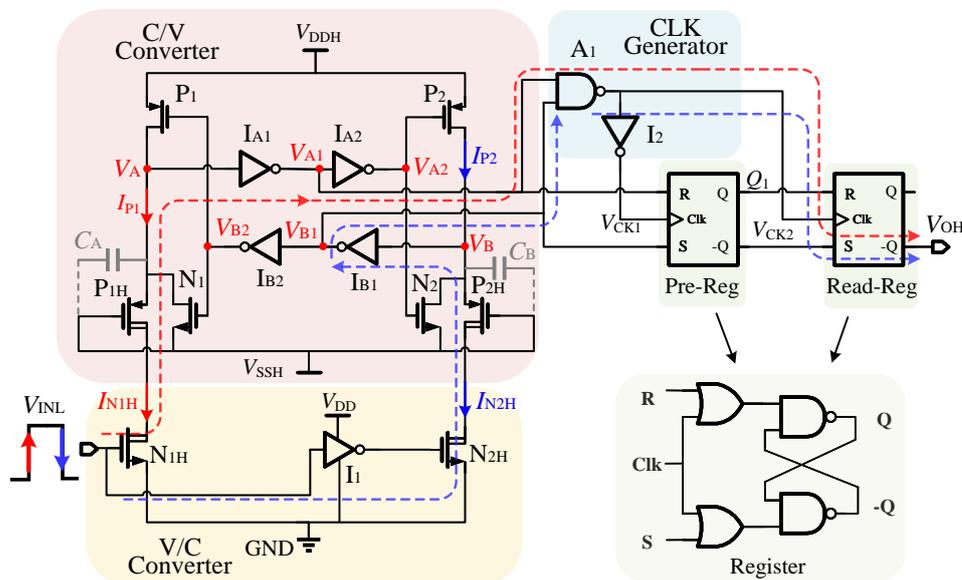


Figure 3. Implementation of the proposed FHV-LS.

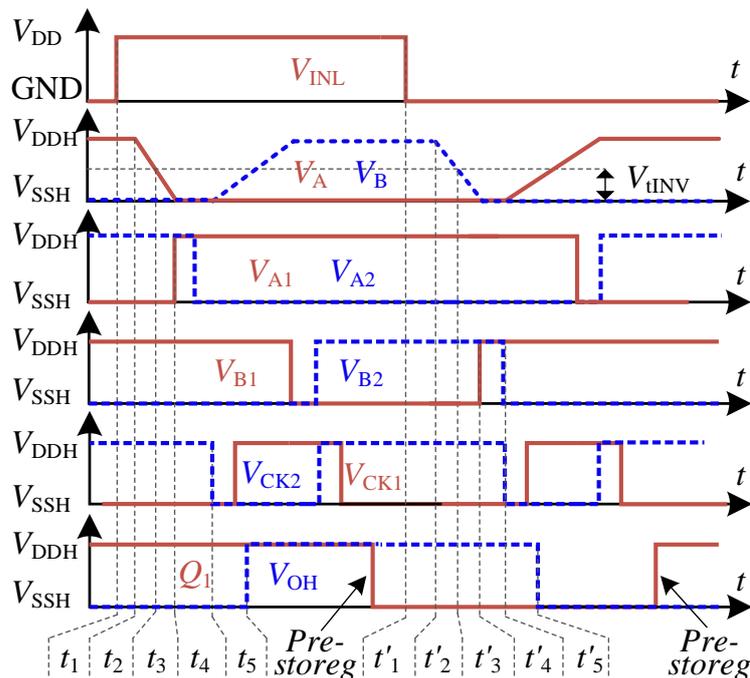


Figure 4. Propagation delay segments of proposed FHV-LS.

When  $V_{INL}$  varies from GND to  $V_{DD}$  rapidly, the signals of FHV-LS are transmitted along with the red dashed line. Firstly,  $N_{1H}$  is turned on, and operates in saturation. Then  $N_{2H}$  is off after the delay of inverter  $I_1$ . To ensure the high-side logic circuits work well, we must succeed in taking  $V_A$  below the threshold  $V_{iINVH}$  of inverter  $I_{A1}$ . It requires that the current  $I_{N1H}/I_{N2H}$  is larger than the current of  $P_1/P_2$  before  $V_A$  falls below  $V_{iINVH}$ . Otherwise, the state of high-side circuits can not be flipped. As voltage  $V_A$  is lower than the threshold of  $I_{A1}$ , the output states of inverter  $I_{A1}$  are reversed. Thus,  $V_{A2} = 0$ , and  $P_2$  is turned on to pull up voltage  $V_B$ . At the beginning,  $V_B$  is lower than the threshold of inverter

$I_{B1}$ ,  $V_{A1} = V_{B1} = 1$ . During this critical time interval,  $V_{CK1} = 1$  and  $V_{CK2} = 0$ . Accordingly, pre-Reg operates in the latch mode while read-Reg in the transfer mode. The state of  $V_{INL} = 1$  stored in the pre-Reg is then transferred to the output of read-Reg. Thus,  $V_{OH} = Q_1 = 1$ . It can be considered that the current input state  $V_{INL} = 1$  is transmitted to  $V_{OH}$  during this period. As voltage  $V_B$  rises above the threshold of inverter  $I_{B1}$ ,  $V_{B1} = 0$ ,  $V_{B2} = 1$ .  $P_1$  is turned off, and  $V_A$  is clamped to floating ground  $V_{SSH}$  by the conducted NMOS  $N_1$ . Then,  $N_{1H}$  goes into linear region to reduce the drain current  $I_{N1H}$ . Due to  $V_{CK1} = 0$ ,  $V_{CK2} = 1$ , pre-Reg operates in the transfer mode, and the read-Reg works in latch-mode. The inputs of pre-Reg are  $V_{A1} = 1$  and  $V_{B1} = 0$ , so  $Q_1 = 0$ . As a result, pre-Reg is loaded with the next state of  $V_{INL}$  again.

When  $V_{INL}$  varies from  $V_{DD}$  to GND rapidly,  $N_{1H}$  is turned off and  $N_{2H}$  is turned on after the delay of inverter  $I_1$ . The signal transmission path is shown as the blue dashed line in Figure 3. Due to the symmetrical circuit structures, the transmission paths are similar. It will not be discussed again.

### 3.3. Propagation Delay Analysis

The propagation delay from  $V_{INL}$  to  $V_{OH}$  can be subdivided into five segments. The segments of the rising and falling propagation delays are depicted in Figure 4. To simplify the expression of equation, we take the following abbreviation:  $V_H = V_{DDH} - V_{SSH}$  and all voltages on the high side are referenced by  $V_{SSH}$ .

Delay  $t_1$  is the transmission time of the V/C converter from  $V_{INL}$  to the current  $I_{N1H}$ . It is determined by the intrinsic delay  $t_{d\_NH}$  of  $N_{1H}/N_{2H}$  which can be minimized using the minimum channel length to decrease the parasitic capacitance. Delay  $t'_1$  is the transmission time from  $V_{INL}$  to  $I_{N2H}$ . Due to the delay  $t_{d\_INV}$  of inverter  $I_1$ , delay  $t'_1$  is longer than  $t_1$ . Thus,  $t_1$  and  $t'_1$  are given by

$$t_1 = t_{d\_NH} \quad (1)$$

$$t'_1 = t_{d\_NH} + t_{d\_INV}. \quad (2)$$

After delay  $t_1$  ( $t'_1$ ),  $N_{1H}$  ( $N_{2H}$ ) is turned on. The parasitic capacitor  $C_A$  ( $C_B$ ) will be discharged to pull down the voltage  $V_A$  ( $V_B$ ). Delay  $t_2$  is the time taken for  $V_A$  ( $V_B$ ) to fall from  $V_H$  to the threshold voltage  $V_{iNVH}$  of inverter  $I_{A1}$  ( $I_{B1}$ ).  $t_2$  is denoted as the fall time. In this delay interval,  $N_{1H}/N_{2H}$  operating in the saturation region is taken as a current source. The current  $I_0$  can be expressed by

$$I_0 = I_{N1,2H} = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right)_{N1,2H} (V_{DD} - V_{iN})^2. \quad (3)$$

Since  $P_1/P_2$  operates in the linear region, it can be treated as a resistance  $R_P$ .

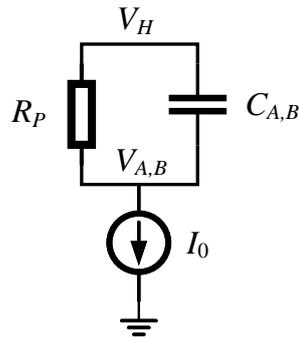
$$R_P = \left[ \mu_p C_{ox} \left( \frac{W}{L} \right)_P (V_H - V_{tp}) \right]^{-1} \quad (4)$$

where  $V_{iN}$  and  $V_{tp}$  are the threshold voltages of  $N_{1H}/N_{2H}$  and  $P_1/P_2$ , respectively.

The equivalent circuit during the fall time of  $V_{A,B}$  is shown in Figure 5. The capacitor  $C_A$  ( $C_B$ ) is the total parasitic capacitance at node  $V_A$  ( $V_B$ ). The equivalent circuit can be regarded as an RC network composed of  $R_P$  and  $C_A$  ( $C_B$ ), which is discharged by the current source  $I_0$ . The RC constant time can be found as  $\tau = C_{A,B} R_P$ . Thus, the voltages can be expressed by

$$V_{A,B}(t) = V_H - I_0 R_P \left( 1 - e^{-t/\tau} \right). \quad (5)$$

It is found from Equation (5) that  $V_{A,B}(t)$  will decrease with the increase of  $t$ . When the time increases to infinity,  $V_{A,B}$  will be close to  $V_H - I_0 R_P$ . In other words,  $V_{A,B}$  will decrease to a lower value with the increase of  $R_P$  under the same time condition.



**Figure 5.** Equivalent circuit during the fall time of  $V_{A,B}$ .

It follows from (5) that the fall time  $t_2$  ( $t'_2$ ) can be derived as

$$t_2 = t'_2 = \tau \ln \left( 1 - \frac{V_H - V_{\text{thNVH}}}{I_0 R_p} \right)^{-1}. \quad (6)$$

To flip the state of inverter  $I_{A1}$  ( $I_{B1}$ ),  $V_A$  ( $V_B$ ) should fall below the threshold voltage  $V_{\text{thNVH}}$  of  $I_{A1}$  ( $I_{B1}$ ). Therefore, the relationship should be satisfied in circuit design

$$I_0 R_p > V_H - V_{\text{thNVH}}. \quad (7)$$

Usually,  $\mu_n = 2\mu_p$  and  $|V_{\text{thN}}| \approx |V_{\text{thP}}|$ . Under the typical condition, we have  $V_{\text{DD}} = V_H$ . Plugging (3) and (4) into (7), the sizes of  $N_{1\text{H}}/N_{2\text{H}}$  and  $P_1/P_2$  should satisfy the following:

$$\left( \frac{W}{L} \right)_{N1,2H} > \frac{V_H - V_{\text{thNV}}}{V_{\text{DD}} - V_{\text{NH}}} \left( \frac{W}{L} \right)_P. \quad (8)$$

As can be seen from (6), the fall time  $t_2$  can be optimized by altering  $V_{\text{thNVH}}$ ,  $I_0$  and  $R_p$  to reduce propagation delay. So, we perform the following arithmetic with  $t_2$ .

$$\frac{\partial t_2}{\partial I_0} = - \frac{R_p C_{A,B} (V_H - V_{\text{thNVH}})}{I_0 [I_0 R_p - (V_H - V_{\text{thNVH}})]} < 0 \quad (9)$$

$$\frac{\partial t_2}{\partial V_{\text{thNVH}}} = - \frac{R_p C_{A,B}}{I_0 R_p - (V_H - V_{\text{thNVH}})} < 0 \quad (10)$$

$$\begin{aligned} \frac{\partial t_2}{\partial R_p} &= C_{A,B} \ln \left[ \frac{I_0 R_p}{I_0 R_p - (V_H - V_{\text{thNVH}})} \right] \\ &\quad - \frac{C_{A,B} (V_H - V_{\text{thNVH}})}{I_0 R_p - (V_H - V_{\text{thNVH}})} \end{aligned} \quad (11)$$

$$\frac{\partial^2 t_2}{\partial R_p^2} = \frac{C_{A,B} (V_H - V_{\text{thNVH}})}{R_p [I_0 R_p - (V_H - V_{\text{thNVH}})]} > 0. \quad (12)$$

It can be concluded from (12) that  $\partial t_2 / \partial R_p$  is positively correlated with  $R_p$ . If we assume  $R_p \rightarrow \infty$ , then  $\partial t_2 / \partial R_p = 0$ . This means that the maximum value of  $\partial t_2 / \partial R_p$  is zero. Thus, the relationship between  $t_2$  and  $R_p$  is

$$\frac{\partial t_2}{\partial R_p} < 0. \quad (13)$$

On the other hand, it can also be seen from Figure 5 that increasing the resistance  $R_p$  can help to accelerate the discharge of the capacitor  $C_{A,B}$ . Therefore, the fall time  $t_2$  of  $V_{A,B}$  will reduce with the increase of  $R_p$ .

As can be observed from (9), (10) and (13), the fall time  $t_2$  is negatively correlated with  $I_0$ ,  $V_{\text{thNVH}}$  and  $R_p$ . In other words, increasing  $I_0$ ,  $V_{\text{thNVH}}$  and  $R_p$  can reduce the fall time  $t_2$ . We can use large-sized devices  $N_{1H}/N_{2H}$  to increase current  $I_0$ , but it will also increase the chip area and power consumption. The threshold voltage  $V_{\text{thNVH}}$  can be raised by enhancing the pull-up ability or by mitigating the pull-down strength of inverter  $I_{A1}/I_{B1}$ . The maximum  $V_{\text{thNVH}}$  can be set close to  $V_H - V_{\text{tp}}$ .  $V_{\text{tp}}$  is the threshold voltage of the PMOS on the high side. Similarly,  $t_2$  ( $t'_2$ ) will decrease with the increase of  $R_p$ , while minimizing the ratio  $W/L$  of  $P_1/P_2$  can increase the pull-up resistance  $R_p$ .

When  $V_A$  ( $V_B$ ) falls below the threshold  $V_{\text{thNVH}}$  of inverter  $I_{A1}$  ( $I_{B1}$ ), voltage  $V_{A1}$  ( $V_{B1}$ ) will be pulled up to high after the delay  $V_{\text{thNVH}}$  of inverter  $I_{A1}$  ( $I_{B1}$ ). Therefore, the delay  $t_3$  ( $t'_3$ ) is the transmission time of inverter  $I_{A1}$  ( $I_{B1}$ ).

$$t_3 = t'_3 = t_{d\_INV}. \quad (14)$$

As  $V_{A1}$  and  $V_{B1}$  are both high,  $V_{\text{CK2}}$  tends to be low after the delay  $t_{d\_Nand}$  of Nand A1. The read-Reg works in transfer-mode, while pre-Reg is in the latch mode. Then the output state of the pre-Reg is transmitted to the output  $V_{\text{OH}}$  after the read-Reg delay  $t_{d\_Reg}$ . The read-Reg is composed of two Nand gates with a cross-coupled connection. Usually, we set delay  $t_{d\_Nand}$  the same as the inverter delay  $t_{d\_INV}$ . Thus, delay  $t_{d\_Reg}$  is twice the delay  $t_{d\_INV}$ . As a result,  $t_4$  and  $t_5$  are expressed by

$$t_4 = t'_4 = t_{d\_Nand} = t_{d\_INV} \quad (15)$$

$$t_5 = t'_5 = t_{d\_Reg} = 2t_{d\_INV}. \quad (16)$$

Thus, the rising propagation delay  $t_{r\_pd}$  from the rising edge of  $V_{\text{INL}}$  to  $V_{\text{OH}}$  is found by

$$\begin{aligned} t_{r\_pd} &= t_1 + t_2 + t_3 + t_4 + t_5 \\ &= t_{d\_NH} + \tau \ln \left( 1 - \frac{V_H - V_{\text{thNVH}}}{I_0 R_p} \right)^{-1} + 4t_{d\_INV}. \end{aligned} \quad (17)$$

Likewise, the fall propagation delay  $t_{f\_pd}$  from the falling edge of  $V_{\text{INL}}$  to  $V_{\text{OH}}$  is found by

$$\begin{aligned} t_{f\_pd} &= t'_1 + t'_2 + t'_3 + t'_4 + t'_5 \\ &= t_{d\_NH} + \tau \ln \left( 1 - \frac{V_H - V_{\text{thNVH}}}{I_0 R_p} \right)^{-1} + 5t_{d\_INV}. \end{aligned} \quad (18)$$

As can be seen from (17) and (18), the propagation delay consists of the intrinsic delay of HV-NMOS, logic gate delay, and  $V_A$  ( $V_B$ ) fall time. Due to the trade-off between power consumption and area, it is quite limited to decrease the intrinsic delay  $t_{d\_NH}$  of MOSFET and the delay  $t_{d\_INV}$  of the logic gate. As can be seen from (13), reduction of the fall time  $t_2$  is a feasible solution to reducing the propagation delay of the proposed FHV-LS. The improvements will be introduced in the next section.

#### 4. Improvements of Proposed FHV-LS

It follows from (13) that the fall time  $t_2$  is negatively correlated with the on-resistance  $R_p$  of  $P_1/P_2$ . During fall time  $t_2$ , the pull-up network  $P_1$  ( $P_2$ ) operating in the linear region has low on-resistance  $R_p$ . It will prolong the discharge time of parasitic capacitance  $C_A/C_B$  at  $V_A/V_B$  node and also increase the fall time  $t_2$ . Hence, an effective solution to reducing the fall time  $t_2$  is to increase  $R_p$ . Comparing (17) and (18), the difference between the rising and falling propagation delays is caused by delay  $t_{d\_INV}$  of the low-side inverter. It will induce a deviation between rising and falling propagation delay. With the decrease in propagation delay, the distortion will increase. In this section, three improvements will be performed to optimize the propagation delay, deviation, and start-up of the proposed

FHV-LS. Simple improvements can be made to the basic design, as shown in Figure 6. In addition, the device parameters of the improved FHV\_LS are summarized in Table 1.

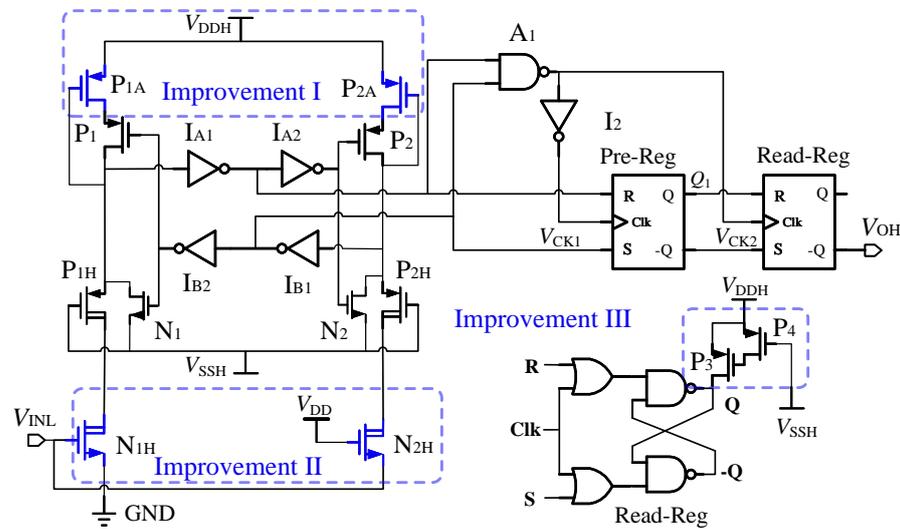


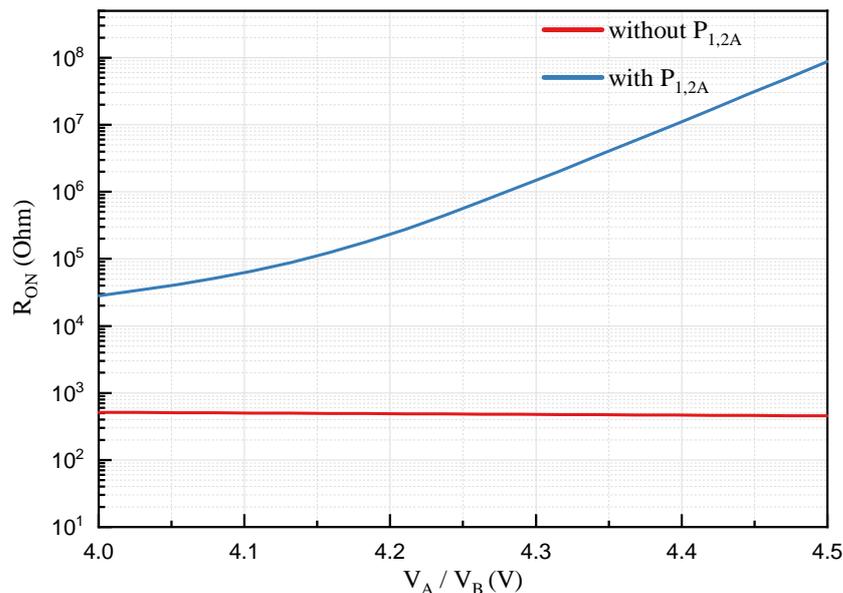
Figure 6. Improvements in propagation delay, symmetry, and startup circuit.

Table 1. Devices parameters of the proposed FHV\_LS.

Devices	$N_{1H}/N_{2H}$	$P_{1H}/P_{2H}$	$N_1/N_2$	$P_1/P_2/P_3/P_4$ $P_{1A}/P_{2A}$	$I_{A1}/I_{B1}$	$I_{A2}/I_{B2}$ $A_1/I_2$	Pre-Reg Read-Reg
W/L ( $\mu\text{m}/\mu\text{m}$ )	40/0.6	24/0.4	10/0.32	10/0.37	N:60/0.32 P:5/0.37	N:10/0.32 P:10/0.37	N:10/0.32 P:20/0.37

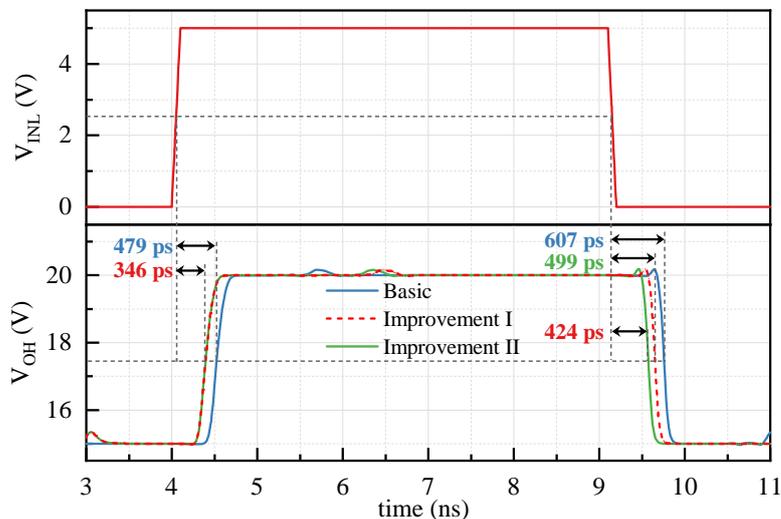
#### 4.1. Improvement-I Reduction of Propagation Delay

To decrease the fall time  $t_2$ , the large on-resistance at the drain of  $P_1/P_2$  is required. For this purpose, a pull-up network with regulated strength [30,31] composed of  $P_1$  ( $P_2$ ) and  $P_{1A}$  ( $P_{2A}$ ) is applied as the improvement-I as depicted in Figure 6. During the fall time  $t_2$  ( $t'_2$ ) interval,  $P_1$  ( $P_2$ ) operates in the linear region, and  $P_{1A}$  ( $P_{2A}$ ) is in sub-threshold region. In addition, maximizing  $V_{\text{INVH}}$  will be able to reduce the fall time  $t_2$ . Thus,  $V_{\text{INVH}}$  is closed to  $V_{\text{DDH}} - V_{\text{th}}$  by selecting the device size of  $I_{A1}$ . The on-resistance of  $P_1$  ( $P_2$ ) and  $P_{1A}$  ( $P_{2A}$ ) is simulated as illustrated in Figure 7. When  $V_{\text{INVH}}$  is set to 4.2 V, the on-resistance  $R_{\text{ON}}$  with  $P_{1A}$  ( $P_{2A}$ ) is two orders of magnitude higher than  $R_{\text{ON}}$  without  $P_1$  ( $P_2$ ), as  $V_A/V_B$  varies between 4.2 V and 5 V, as shown in Figure 7. The resistance  $R_P$  of the regulated strength pull-up network is higher than the resistance of  $P_{1A}$  ( $P_{2A}$ ). Therefore, the fall time  $t_2$  and propagation delay of proposed FHV-LS will be decreased by the pull-up network with the regulated strength. Due to the reduction in pull-up capacity of the pull-up network with the regulated strength, the rise time of  $V_{A,B}$  will increase. Fortunately, the propagation delay of the proposed FHV-LS is independent of the rise time of  $V_A/V_B$  since the pre-storage technique optimizes the transmission path. Compared with traditional resistance enhancement techniques (replace  $P_{1A}/P_{2A}$  with passive resistors), the pull-up network with the regulated strength can achieve a better trade-off between propagation delay, power consumption, and chip area.



**Figure 7.** On-resistance of  $P_1$  ( $P_2$ ) with and without  $P_{1A}$  ( $P_{2A}$ ).

The post-layout simulation with Improvement-I is performed to verify the reduction in propagation delay as depicted in Figure 8. Compared with the basic proposed FHV-LS, the rising propagation delay with Improvement-I decreases from 479 ps to 346 ps, and the fall propagation delay drops from 607 ps to 499 ps. In other word, the average propagation delay is reduced by 22%.



**Figure 8.** Simulation on the propagation delay with Improvement-I and Improvement-II.

#### 4.2. Improvement-II Optimizing the Symmetry of Propagation Delay

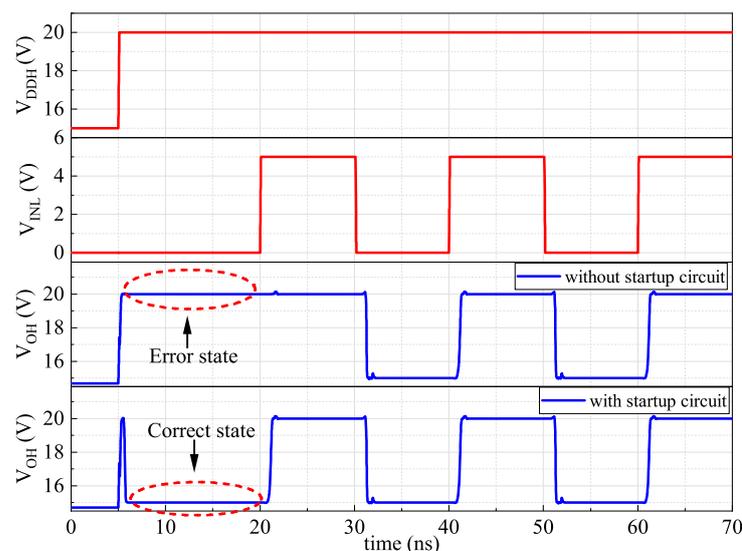
The deviation between the rising and falling propagation delays is induced by the transmission delay of inverter  $I_1$  on the low side. The common-gate structure is introduced to replace the low-side inverter as Improvement-II [32,33], as shown in Figure 6. The source terminal of  $N_{2H}$  is connected to  $V_{INL}$  directly, forming a pseudosymmetry input pair. The input of  $N_{1H}$  is the gate, while the input of  $N_{2H}$  is the source.  $V_{INL}$  is the common input signal of  $N_{1H}$  and  $N_{2H}$ . The switching processes of  $N_{1H}$  and  $N_{2H}$  are almost simultaneous. From another perspective, the left and right branches of the proposed FHV-LS are quasi-symmetrical structurally. As a result, the deviation between rising and falling propagation delay will be reduced. However, the transistor  $N_{2H}$  exhibits body effect as the source/body

is separated. With the same size, the intrinsic delay of  $N_{2H}$  is longer than that of  $N_{1H}$ . Compared with the inverter delay, this difference is very small.

The post-layout simulation with Improvement-II is performed to verify the reduction in deviation between the rising and falling propagation delays in Figure 8. The falling propagation delay decreases from 499 ps to 424 ps, while the rising propagation delay is unchanged. The reduction in falling propagation delay is attributed to the introduction of the quasi-symmetrical input to replace the inverter on the low side. The deviation between rising and falling propagation delay decreases from 36% to 20%. The difference between the rising and falling propagation delays is 75 ps which is caused by the body effect of  $N_{2H}$ .

#### 4.3. Improvement-III Start-Up Circuit

When  $V_{DDH}$  is powered up, the output of the proposed FHV-LS is a uncertain state due to the read-Reg in latch mode. To overcome this problem, a start-up circuit composed of  $P_3/P_4$  is developed to initialize the state of the read-Reg, as shown in Figure 6. During  $V_{DDH}$  power-up, the current of  $P_3$  pulls the Q of read-Reg to high. Consequently,  $V_{OH}$  is low. Then  $P_3$  is turned off by  $P_4$ . There is no quiescent current consumption on  $P_3/P_4$  after  $V_{DDH}$  power-up. The outputs of read-Reg with and without the start-up circuit are simulated in Figure 9. In case of no start-up circuit, the output  $V_{OH}$  of read-Reg is high after  $V_{DDH}$  power-up. It is an error state, which is not in agreement with input  $V_{INL}$ . With the start-up circuit, the  $V_{OH}$  is pulled down after  $V_{DDH}$  power-up. As a result, the  $V_{OH}$  follows the input  $V_{INL}$  correctly under any operating conditions.



**Figure 9.** The output state of proposed FHV-LS with and without the start-up circuit during  $V_{DDH}$  power-up.

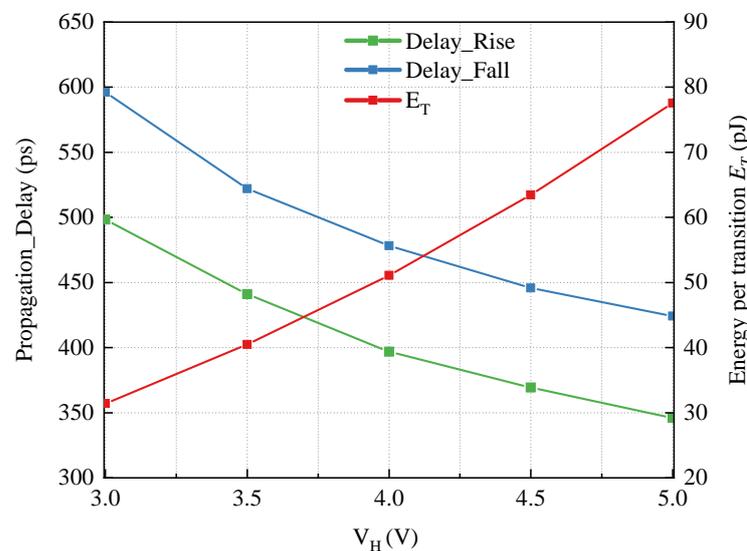
## 5. Post-Layout Simulation

To comprehensively evaluate the performance of the proposed FHV\_LS, post-layout simulations are performed for the propagation delay, power consumption, and stability. The simulation tool used for this work is Cadence Spectre Simulator (Cadence Design Systems, Inc., San Jose, CA, USA), version 6.17. In addition, the design and verification tools for the layout of this work are Cadence Virtuoso Layout Suite (Cadence Design Systems, Inc., San Jose, CA, USA) and Mentor Graphics Calibre (Mentor Graphics Corporation, Plano, TX, USA), respectively.

### 5.1. Supply Voltage Simulation

The average propagation delay and power consumption versus supply voltage  $V_H$  are exhibited in Figure 10. As  $V_H$  varies from 3 V to 5 V, the rising propagation delay

changes from 498 ps to 346 ps and the falling propagation delay changes from 596 ps to 424 ps, while the  $E_T$  changes from 31.5 pJ to 77.5 pJ. From Equations (17) and (18), it is known that the propagation delays consist of the delays of logic gates and the fall time of  $V_{A,B}$ , which are nonlinear with respect to the supply voltage, taking Equations (3) and (4) into condition. Therefore, there is a nonlinear relationship between the propagation delay and supply voltage. On the other hand, the delay of logic gates, as can be seen from Equations (17) and (18), is the major component in the propagation delay. Based on the principle of integrated circuit, the propagation delay of logic gates decreases as the supply voltage increases. As a result, it can be found from Figure 10 that the propagation delays of proposed FHV-LS are negatively correlated with the supply voltage. To achieve low propagation delay, higher supply voltage is required, but power consumption is increased as well. In addition, the rising propagation delay is lower than falling propagation delay since the body effect exists in the input device  $N_{2H}$ . With Improvement-II, the deviation between rising and falling propagation is lower than 17%.



**Figure 10.** Simulation of the propagation delay and energy per transition ( $E_T$ ) versus power supply  $V_H$ .

### 5.2. Process Corners Simulation

The propagation delay and  $E_T$  at different process corners are simulated in Figure 11. The rising and falling propagation delay at typical process corner are 346 ps and 424 ps, respectively. Based on the typical process corner, the drift value on propagation delay at ss and ff corners is lower than 15%, and the drift value on propagation delay at fs and sf process corners is lower than 2.5%. As can be seen from Figure 11, the maximum power consumption of  $E_T$  appears at the fs corner. At this corner, the logic threshold of  $I_{A1}$  is lower than that of other corners. As a result, the dynamic power consumption of  $I_{A1}$  at the fs corner will increase. Conversely, the dynamic power consumption of  $I_{A1}$  at the sf corner will decrease for the higher logic threshold, since the logic thresholds at tt/ff/ss corners are almost unchanged, and they also have similar energy per transition ( $E_T$ ).

### 5.3. Temperature Simulation

The simulation of the propagation delay and  $E_T$  at different temperature are shown in Figure 12. As temperature varies from  $-40$  °C to  $125$  °C, the rising and falling propagation delays increase from 307 ps to 402 ps and from 374 ps to 501 ps, respectively. Therefore, the temperature coefficients of the rising and falling propagation delay are  $0.75$  ps/°C and  $0.56$  ps/°C, respectively. As can be seen from the figure,  $E_T$  is positively correlated with the temperature as well. The temperature coefficient of  $E_T$  is  $0.024$  pJ/°C.

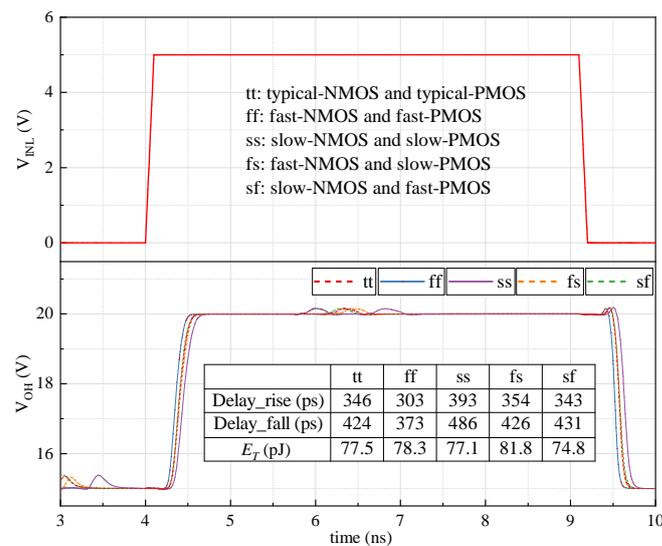


Figure 11. Simulations on the propagation delay and  $E_T$  at different process corners.

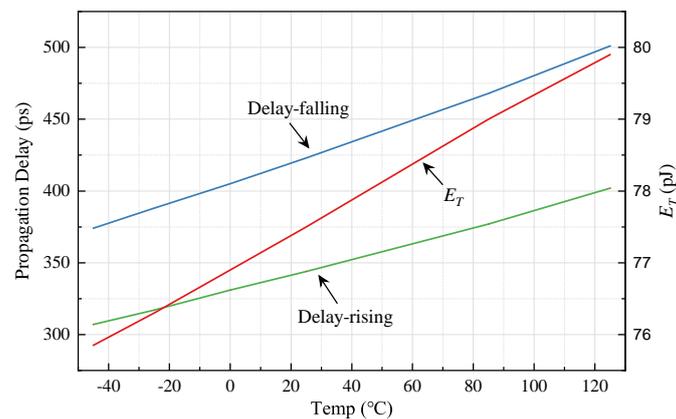


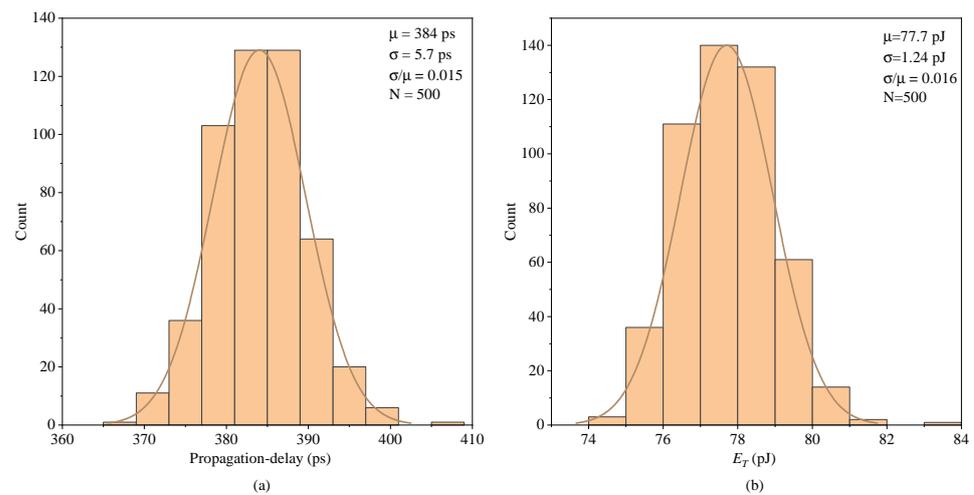
Figure 12. Propagation delay and  $E_T$  versus temperature simulation.

#### 5.4. Monte Carlo Simulation

To study the variation against the device mismatch and process, 500-point Monte Carlo simulations on the propagation delay and  $E_T$  of the proposed FHV-LS are carried out in Figure 13. The simulation conditions are  $V_{DDH} = 20$  V,  $V_{SSH} = 15$  V,  $V_{DD} = 5$  V, and  $f_{VINL} = 1$  MHz. With statistical analysis, the means of the propagation delays and  $E_T$  are 384 ps and 77.7 pJ, respectively. Their normalized standard deviations ( $\sigma/\mu$ ) are 0.015 and 0.016, respectively. As can be seen from the simulation results, the propagation delay and  $E_T$  have good stability against process variation and devices mismatch.

#### 5.5. Discussion

To reduce the propagation delay, a pull-up network with regulated strength is applied to increase the pull-up resistance. The advantage of Improvement I is that the fall time of  $V_A/V_B$  is reduced. On the one hand, the rise time of  $V_A/V_B$  is increased due to the large pull-up resistance. As a result, the maximum operating frequency should not exceed 100 MHz for the proposed FHV-LS. However, the operating frequency of insulated gate bipolar transistor (IGBT) and SiC power devices are lower than 10 MHz. Therefore, the frequency of 100 MHz is enough for the applications. On the other hand, the immunity for  $dV/dt$  of  $V_{SSH}$  is reduced compared with the basic proposed FHV-LS. The maximum immunity for  $dV/dt$  of  $V_{SSH}$  is 5 V/ns. Therefore, the proposed FHV-LS is appropriate for the application of half-bridge with low  $dV/dt$  or the half-bridge consisting of CMOS structure.



**Figure 13.** Monte Carlo simulation: (a) Average propagation delay, (b)  $E_T$ .

Table 2 summarizes the performance of the proposed LS and previous works. The process, supply voltage, propagation delay,  $E_T$ , area, and figure of merit (FoM and FoM\*) are listed in the table. The average propagation delay of the proposed FHV-LS is 384 ps using 0.32  $\mu\text{m}$  HVC MOS technology. In addition, FoM from [16] and FoM\* from [20] are 0.06 and 38, respectively. The low propagation delay of this work mainly benefits from the pre-storage technique and the pull-up network with regulated strength. Specifically, the pre-storage technique decreases the number of delay units along the signal transmission path from  $V_{\text{INL}}$  to  $V_{\text{OH}}$ , leading to optimal transmission paths. To reduce the major delay  $t_2$  in the propagation delay, a pull-up network with regulated strength is employed to increase the pull-up resistance  $R_p$ . Consequently, the proposed FHV-LS features low propagation delay and FoM, as shown in Table 2. In addition, the propagation delay can be optimized according to the analysis of the propagation delay. Based on the operating mechanism of the integrated circuit, the power consumption can be reduced by increasing the propagation delay. In accordance with application requirements, the propagation delay and power consumption of the proposed FHV-LS can be optimized to achieve the trade-off.

**Table 2.** Comparison with previous work.

	Process $\mu\text{m}$	Voltage V	Delay ns	$E_T$ pJ	Area $\mu\text{m}^2$	FoM	FoM*	
[15]	0.5	30	1.7	NA	6500	0.11	NA	Measured
	HVC MOS							
[16]	0.5	40	1.7	NA	NA	0.09	NA	Measured
	HVC MOS							
[17]	0.35	20	2.4	24	NA	0.34	67	Measured
	HVC MOS							
[20]	0.18	20	0.37	7.2	4849	0.1	23	Measured
	HVC MOS							
[21]	0.18	50	0.53	30.3	17595	0.06	54	Measured
	HVC MOS							
[25]	0.3	23	1.34	NA	NA	0.19	NA	Measured
	HVC MOS							
[26]	0.18	40	1.4	4.1	7350	0.19	20.4	Measured
	HVC MOS							
[28]	0.18	50	0.5	NA	NA	0.06	NA	Simulated
	BCD							
This work	0.32	20	0.38	77.7	36406	0.06	38	Simulated
	HVC MOS							

FoM from [16]: (Delay)/(Process·Voltage). Unit: ns/( $\mu\text{m}\cdot\text{V}$ ); FoM\* from [20]: ( $E_T\cdot\text{Delay}$ )/(Process<sup>3</sup>·Voltage). Unit: (pJ·ns)/( $\mu\text{m}^3\cdot\text{V}$ ).

## 6. Conclusions

In this paper, a novel FHV-LS with pre-storage technique is proposed to achieve low propagation delay. In the steady state, the input state of FHV-LS is stored in a register. As soon as the input starts switching, the state stored in the register is transmitted to the output of FHV-LS under the control of the CLK generator. Thus, the propagation delay of the proposed FHV-LS is reduced to the sub-nanosecond scale. Since the fall time  $t_2$  in propagation delay is inversely correlated with the pull-up resistance  $R_P$ , a pull-up network with the regulated strength is used to increase the pull-up resistance  $R_P$ . Therefore, the average propagation delay reduces. To reduce the deviation between rising and falling propagation delay, a pseudosymmetry input pair is introduced to improve the symmetry of the proposed FHV-LS structurally. Moreover, a start-up circuit is designed to initialize the output state of FHV-LS during power-up. Post-layout simulation indicates that the average propagation delay and  $E_T$  of the proposed FHV-LS are 384 ps and 77.7 pJ at  $V_H = 5$  V. Monte Carlo simulation results demonstrate that the proposed FHV-LS has good stability against process variation and devices mismatch.

**Author Contributions:** Data curation, H.M. and G.Y.; Formal analysis, Q.L.; Investigation, Y.Z.; Methodology, Q.L.; Project administration, Y.Y.; Software, G.Y. and M.Z.; Writing—review and editing, Y.Y. and W.X. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research was funded by National Natural Science Foundation of China, grant number 62174134. And Shaanxi Innovation Capability Support Project, grant number 2021TD-25.

**Institutional Review Board Statement:** Not applicable.

**Informed Consent Statement:** Not applicable.

**Data Availability Statement:** Not applicable.

**Conflicts of Interest:** The authors declare no conflict of interest.

## References

1. Riazmontazer, H.; Mazumder, S.K. Optically Switched-Drive-Based Unified Independent  $dv/dt$  and  $di/dt$  Control for Turn-Off Transition of Power MOSFETs. *IEEE Trans. Power Electron.* **2015**, *30*, 2338–2349. [[CrossRef](#)]
2. Ling, Y.; Zhao, Z.; Zhu, Y. A Self-Regulating Gate Driver for High-Power IGBTs. *IEEE Trans. Power Electron.* **2021**, *36*, 3450–3461. [[CrossRef](#)]
3. Chen, H.Y.; Kao, Y.Y.; Zhang, Z.Q.; Liao, C.H.; Yang, H.Y.; Hsu, M.S.; Chen, K.H.; Lin, Y.H.; Lin, S.R.; Tsai, T.Y. 33.1 A Fully Integrated GaN-on-Silicon Gate Driver and GaN Switch with Temperature-compensated Fast Turn-on Technique for Improving Reliability. In Proceedings of the 2021 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 13–22 February 2021; pp. 460–462. [[CrossRef](#)]
4. Camacho, A.P.; Sala, V.; Ghorbani, H.; Martinez, J.L.R. A Novel Active Gate Driver for Improving SiC MOSFET Switching Trajectory. *IEEE Trans. Ind. Electron.* **2017**, *64*, 9032–9042. [[CrossRef](#)]
5. Yang, Y.; Wen, Y.; Gao, Y. A Novel Active Gate Driver for Improving Switching Performance of High-Power SiC MOSFET Modules. *IEEE Trans. Power Electron.* **2019**, *34*, 7775–7787. [[CrossRef](#)]
6. Wen, Y.; Yang, Y.; Gao, Y. Active Gate Driver for Improving Current Sharing Performance of Paralleled High-Power SiC MOSFET Modules. *IEEE Trans. Power Electron.* **2021**, *36*, 1491–1505. [[CrossRef](#)]
7. Sun, K.; Wang, J.; Burgos, R.; Boroyevich, D. Design, Analysis, and Discussion of Short Circuit and Overload Gate-Driver Dual-Protection Scheme for 1.2-kV, 400-A SiC MOSFET Modules. *IEEE Trans. Power Electron.* **2020**, *35*, 3054–3068. [[CrossRef](#)]
8. Nevarez, J.; Olmedo, A.; Williams, R.; Pechnikova, P. Gate Driver Protection Methods for SiC MOSFET Short Circuit Testing. In Proceedings of the 2021 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 21–25 March 2021; pp. 1–4. [[CrossRef](#)]
9. Seidel, A.; Wicht, B. Integrated Gate Drivers Based on High-Voltage Energy Storing for GaN Transistors. *IEEE J. Solid-State Circuit* **2018**, *53*, 3446–3454. [[CrossRef](#)]
10. Zhang, W.J.; Yu, J.; Cui, W.T.; Leng, Y.; Liang, J.; Hsieh, Y.T.; Tsai, H.H.; Juang, Y.Z.; Yeh, W.K.; Ng, W.T. A Smart Gate Driver IC for GaN Power HEMTs with Dynamic Ringing Suppression. *IEEE Trans. Power Electron.* **2021**, *36*, 14119–14132. [[CrossRef](#)]
11. Zhang, Z.; Dix, J.; Wang, F.; Blalock, B.J.; Costinett, D.; Tolbert, L.M. Intelligent Gate Drive for Fast Switching and Crosstalk Suppression of SiC Devices. *IEEE Trans. Power Electron.* **2017**, *32*, 9319–9332. [[CrossRef](#)]
12. Rouger, N.; Barazi, Y.; Cousineau, M.; Richardeau, F. Modular Multilevel SOI-CMOS Active Gate Driver Architecture for SiC MOSFETs. In Proceedings of the 2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Vienna, Austria, 13–18 September 2020; pp. 278–281. [[CrossRef](#)]

13. Kobayashi, K.; Yanagigawa, H.; Mori, K.; Yamanaka, S.; Fujiwara, A. High voltage SOI CMOS IC technology for driving plasma display panels. In Proceedings of the 10th International Symposium on Power Semiconductor Devices and ICs. ISPSD'98 (IEEE Cat. No.98CH36212), Kyoto, Japan, 3–6 June 1998; pp. 141–144. [\[CrossRef\]](#)
14. Choi, B.D. Enhancement of current driving capability in data driver ICs for plasma display panels. *IEEE Trans. Consum. Electron.* **2009**, *55*, 992–997. [\[CrossRef\]](#)
15. Li, Y.; Wen, C.; Yuan, B.; Wen, L.; Ye, Q. A high speed and power-efficient level shifter for high voltage buck converter drivers. In Proceedings of the 2010 10th IEEE International Conference on Solid-State and Integrated Circuit Technology, Shanghai, China, 1–4 November 2010; pp. 309–311. [\[CrossRef\]](#)
16. Liu, Z.; Cong, L.; Lee, H. Design of On-Chip Gate Drivers with Power-Efficient High-Speed Level Shifting and Dynamic Timing Control for High-Voltage Synchronous Switching Power Converters. *IEEE J. Solid-State Circuits* **2015**, *50*, 1463–1477. [\[CrossRef\]](#)
17. Moghe, Y.; Lehmann, T.; Piessens, T. Nanosecond Delay Floating High Voltage Level Shifters in a 0.35  $\mu\text{m}$  HV-CMOS Technology. *IEEE J. Solid-State Circuits* **2011**, *46*, 485–497. [\[CrossRef\]](#)
18. Ming, X.; Zhang, X.; Zhang, Z.W.; Feng, X.D.; Hu, L.; Wang, X.; Wu, G.; Zhang, B. A high-voltage half-bridge gate drive circuit for GaN devices with high-speed low-power and high-noise-immunity level shifter. In Proceedings of the 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Chicago, IL, USA, 13–17 May 2018; pp. 355–358. [\[CrossRef\]](#)
19. Buyle, J.; De Gezelle, V.; Bakeroot, B.; Doutreloigne, J. A new type of level-shifter for n-type high side switches used in high-voltage switching ADSL line-drivers. In Proceedings of the 2008 15th IEEE International Conference on Electronics, Circuits and Systems, Saint Julian's, Malta, 31 August–3 September 2008; pp. 954–957. [\[CrossRef\]](#)
20. Liu, D.; Hollis, S.J.; Dymond, H.C.P.; McNeill, N.; Stark, B.H. Design of 370-ps Delay Floating-Voltage Level Shifters With 30-V/ns Power Supply Slew Tolerance. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2016**, *63*, 688–692. [\[CrossRef\]](#)
21. Liu, D.; Hollis, S.J.; Stark, B.H. A New Design Technique for Sub-Nanosecond Delay and 200 V/ns Power Supply Slew-Tolerant Floating Voltage Level Shifters for GaN SMPS. *IEEE Trans. Circuits Syst. I Reg. Pap.* **2019**, *66*, 1280–1290. [\[CrossRef\]](#)
22. Ma, H.; Namgoong, G.; Choi, E.; Bien, F. Instantaneous Power Consuming Level Shifter for Improving Power Conversion Efficiency of Buck Converter. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2019**, *66*, 1207–1211. [\[CrossRef\]](#)
23. Li, F.; Giannopoulos, D.; Wacyk, I. A low loss high-frequency half-bridge driver with integrated power devices using EZ-HV SOI technology. In Proceedings of the APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335), Dallas, TX, USA, 10–14 March 2002; pp. 1127–1132. [\[CrossRef\]](#)
24. Zhu, J.; Zhang, Y.; Sun, W.; Lu, Y.; Shi, L.; Gu, Y.; Zhang, S. Noise Immunity and its Temperature Characteristics Study of the Capacitive-Loaded Level Shift Circuit for High Voltage Gate Drive IC. *IEEE Trans. Ind. Electron.* **2018**, *65*, 3027–3034. [\[CrossRef\]](#)
25. Yuan, B.; Ying, J.; Ng, W.T.; Lai, X.Q.; Zhang, L.F. A High-Voltage DC–DC Buck Converter With Dynamic Level Shifter for Bootstrapped High-Side Gate Driver and Diode Emulator. *IEEE Trans. Power Electron.* **2020**, *35*, 7295–7304. [\[CrossRef\]](#)
26. Lutz, D.; Seidel, A.; Wicht, B. A 50V, 1.45ns, 4.1pJ High-Speed Low-Power Level Shifter for High-Voltage DCDC Converters. In Proceedings of the ESSCIRC 2018—IEEE 44th European Solid State Circuits Conference (ESSCIRC), Dresden, Germany, 3–6 September 2018; pp. 126–129. [\[CrossRef\]](#)
27. Liu, Z.; Lee, H. A 100V gate driver with sub-nanosecond-delay capacitive-coupled level shifting and dynamic timing control for ZVS-based synchronous power converters. In Proceedings of the IEEE 2013 Custom Integrated Circuits Conference, San Jose, CA, USA, 22–25 September 2013; pp. 1–4. [\[CrossRef\]](#)
28. Salimath, A.; Gonano, G.; Bonizzoni, E.; Brambilla, D.; Botti, E.; Maloberti, F. A high-speed level shifting technique and its application in high-voltage, synchronous DC-DC converters with quasi-ZVS. In Proceedings of the 2017 IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, MD, USA, 28–31 May 2017; pp. 1–4. [\[CrossRef\]](#)
29. Abdelmoaty, A.; Al-Shyoukh, M.; Fayed, A. A high-voltage level shifter with sub-nano-second propagation delay for switching power converters. In Proceedings of the 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 20–24 March 2016; pp. 2437–2440. [\[CrossRef\]](#)
30. Lanuzza, M.; Corsonello, P.; Perri, S. Low-Power Level Shifter for Multi-Supply Voltage Designs. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2012**, *59*, 922–926. [\[CrossRef\]](#)
31. Kabirpour, S.; Jalali, M. A Low-Power and High-Speed Voltage Level Shifter Based on a Regulated Cross-Coupled Pull-Up Network. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2019**, *66*, 909–913. [\[CrossRef\]](#)
32. Le, V.L.; Kim, T.T.H. An Area and Energy Efficient Ultra-Low Voltage Level Shifter With Pass Transistor and Reduced-Swing Output Buffer in 65-nm CMOS. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2018**, *65*, 607–611. [\[CrossRef\]](#)
33. Kabirpour, S.; Jalali, M. A Power-Delay and Area Efficient Voltage Level Shifter Based on a Reflected-Output Wilson Current Mirror Level Shifter. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2020**, *67*, 250–254. [\[CrossRef\]](#)