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An Enhanced Threshold Voltage Model of MOSFETs for the 6-300 K Temperature Range

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Abstract

An enhanced threshold voltage model for MOSFETs over a wide range of temperature from 6 K to 300 K is presented. The model takes into account the carrier freeze-out effect and the external field-assisted ionization to address the temperature dependence of MOS transistors. For simplicity, an empirical function is incorporated to predict short channel effects over the temperature range. The results from the proposed model demonstrate good agreement with NMOS and PMOS transistors measured from fabricated chips.

Keywords: Cryogenic Electronics, Threshold Voltage, MOSFETs.

1. Introduction

The demand for deploying MOS circuits in extreme environments has recently increased with the inevitability of low temperature applications such as space exploration and quantum computing [1]. Devices operating at reduced temperatures show abnormal behaviour caused by effects such as carrier freeze-out, which strongly impact circuit performance [2, 3].

One of the key parameters in conventional MOSFET models is the threshold voltage, which is an essential quantity in MOSFET circuit design and an effective quality control indicator when evaluating device reliability [4]. Several works have mentioned the increase of the threshold voltage when temperature decreases mainly due to the change of Fermi potential [2, 3, 5–11]. Some attempts have been made to create low temperature MOS models, in which the threshold voltage at room temperature is replaced by its cold value [6, 7], or by polynomial fitting functions [8, 10]. Models devised for a specific temperature may need to be characterized at that temperature, and might not provide insight into the device behaviour over a wide temperature range. In addition, the complexity of the fitting function needs to be considered to achieve high computational efficiency. Therefore, a simplified threshold voltage model that faithfully accounts for wide changes in the temperature should be developed.

This work presents the first threshold voltage model for bulk CMOS transistors over the 6–300 K temperature range. We propose a simplified Fermi potential formula, which takes into account the freeze-out effect and the external field-assisted ionization. The short channel effect as a function of temperature is also presented.

2. Temperature dependencies of Threshold voltage

2.1. N-channel devices

Threshold voltage is defined as a value of the gate voltage when the substrate immediately underneath starts to be inverted, forming a carrier channel between the source and drain. In a long N-channel device at zero substrate bias, the threshold voltage is given as [11]

$$V_{th0} = V_{FB} + \phi_0 + \gamma\sqrt{\phi_0}\,, \tag{1}$$

where V_{FB} is the flat-band voltage, γ is the body-effect coefficient, and ϕ_0 is the surface potential. Also, $V_{FB} = -|\phi_F| - \phi_{gate} - \frac{Q'_o}{C'_{ox}}$, where $|\phi_F|$ is the Fermi potential, ϕ_{gate} is the work function of the gate, Q'_o represents the effective oxide charge per unit area, and C'_{ox} is the gate capacitance per unit area. In strong inversion $\phi_0 \approx 2|\phi_F|$, thus Eq. (1) becomes

$$V_{th0} = |\phi_F| - \phi_{gate} - \frac{Q'_o}{C'_{ox}} + \gamma\sqrt{2|\phi_F|}\,. \tag{2}$$

In Eq. (2), ϕ_{gate} has almost no temperature dependence due to the gate being degenerately doped [2], and $\frac{Q'_o}{C'_{ox}}$ can be assumed constant in strong inversion [7].

The conventional formula used to calculate the Fermi potential is $\phi_F = \frac{k_B T}{q}\ln(\frac{N_A}{n_i})$, where k_B is Boltzmann's constant, q is the elementary charge, n_i is the intrinsic concentration and N_A is the substrate doping concentration which is assumed equal to the ionized acceptor concentration N_A^- at room temperature. However, for a wide temperature range and especially at low temperatures where N_A^- is no longer equal to N_A due to the freeze-out effect, N_A^- is modelled as $N_A^- = \frac{N_A}{1+4e^{(E_A-E_F)/k_BT}}$ (Fig. 1(a)) [12].

In this paper, the Fermi potential ϕ_F, used in Fermi-Dirac statistics, is derived from the Fermi energy instead of carrier concentrations as $\phi_F = \frac{E_F - E_i}{q}$, where E_i is the intrinsic energy and E_F is the Fermi energy [11]. Taking into account the freeze-out of acceptors and solving for the Fermi energy in the charge neutrality condition for p-type material [2], the Fermi potential

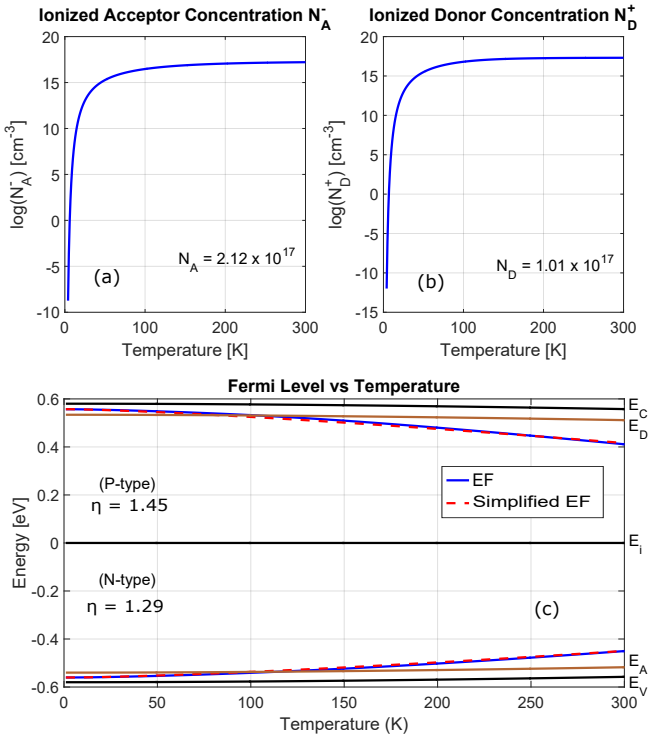

Figure 1: (a) Ionized Acceptor concentration N_A^-, (b) Ionized Donor concentration N_D^+, and (c) Simplified model of Fermi energy E_F.

ϕ_F is expressed as

$$\phi_F = \frac{E_A + E_V}{2q} - \frac{k_B T}{2q} ln\left(\frac{N_A}{4N_V}\right) - \frac{k_B T}{q} sinh^{-1}\left(\sqrt{\frac{N_V}{16N_A}} e^{-(E_A - E_V)/2k_B T}\right), \quad (3)$$

where $N_V \approx 2.0015{\times}10^{15}{\times}T^{3/2}$ is the effective density of states in the valence band for Si, and E_A and E_V are the energy level of acceptor and valence band, respectively [12]. Note that all energy levels are referenced to the intrinsic energy. Eq. (3) can be simplified by introducing the fitting parameter, η, and neglecting the inverse hyperbolic sine term to obtain

$$\phi_F \cong \frac{E_A + E_V}{2q} - \frac{\eta k_B T}{2q} ln\left(\frac{N_A}{4N_V}\right). \quad (4)$$

This simplification makes ϕ_F less computationally expensive and facilitates incorporating it into SPICE models. The difference between the simplified ϕ_F in Eq. (4) versus the one in Eq. (3) is less than one percent. A plot of ϕ_F or E_F referenced to E_i = 0 is shown in Fig. 1(c).

The other factor that must be taken into account at low temperatures is field-assisted or Poole-Frenkel ionization [13]. This mechanism reveals that when a field is applied, the potential barrier moves lower meaning that the field assists carrier ionization. The reduction of the potential barrier due to an applied field can be determined as $\Delta U{=}2\sqrt{\frac{qF}{\varepsilon_{Si}}}$, where F is the field strength, and ε_{Si} is the permittivity of silicon [13]. Based on the Poole-Frenkel theory, we define $\Delta\phi_G$ as the potential reduction caused by the external field or the gate voltage ΔV_G. Therefore, $\Delta\phi_G$ can be given as

$$\Delta\phi_G = 2\sqrt{\frac{q\Delta V_G}{\varepsilon_{Si} T_{ox}}}, \quad (5)$$

where T_{ox} is the gate oxide thickness.

Since low temperatures lead to freeze-out of carriers, a sufficient field is required to assist the ionization of trapped carriers, depletion region formation, and channel formation. We propose a formula to calculate the potential change required to ionize and form the channel as follows

$$\frac{\Delta\phi_G}{k_B T} = \beta\left(\frac{\phi_{AF0}}{k_B T_0} - \frac{\phi_{AF}}{k_B T}\right), \quad (6)$$

where β is an empirical constant which is proportional to the amount of potential reduction. Here, ϕ_{AF} is the activation potential for acceptors defined as

$$\phi_{AF} = \frac{E_A - mE_F}{q}, \quad (7)$$

where m is a freeze-out coefficient corresponding to the strong freeze-out effect (this point will be discussed later). Also, ϕ_{AF0} is the activation potential at room temperature T_0. Eq. (6) shows the amount of potential required to assist carrier ionization, and form the channel at the level of carrier concentration for room temperature.

From (5) and (6), ΔV_G corresponding to the potential reduction $\Delta\phi_G$ can be determined as

$$\Delta V_G = \frac{\varepsilon_{Si} T_{ox}}{4q}\beta^2\left(\phi_{AF0}\frac{T}{T_0} - \phi_{AF}\right)^2. \quad (8)$$

Therefore, the threshold voltage formula for a wide range of temperatures can be rewritten as

$$V_{th0} = |\phi_F| - \phi_{gate} - \frac{Q'_o}{C'_{ox}} + \gamma\sqrt{2|\phi_F|} + \Delta V_G. \quad (9)$$

2.2. P-channel devices

Similar to the N-channel devices, the threshold voltage model of P-channel devices over 6-300 K temperature range can be written as

$$V_{th0} = \phi_F - \phi_{gate} - \frac{Q'_o}{C'_{ox}} + \gamma\sqrt{2\phi_F} + \Delta V_G, \quad (10)$$

where

$$\phi_F \cong \frac{E_D + E_C}{2q} + \frac{\eta k_B T}{2q} ln\left(\frac{N_D}{2N_C}\right). \quad (11)$$

In Eq. (11), E_D and E_C are the energy levels of donors and conduction band, respectively [12]. $N_C \approx 5.4078{\times}10^{15}{\times}T^{3/2}$ is the effective density of states in the conduction band for Si. The ionized donors are given as $N_D^+ = \frac{N_D}{1+2e^{(E_F - E_D)/k_B T}}$ [12], where N_D is the donor concentration (Fig. 1(b)).

The additional field-assisted ionization ΔV_G for the P-channel devices also follows the proposed formula in Eq. (8) with the activation potential ϕ_{AF} given as

$$\phi_{AF} = \frac{E_D - mE_F}{q} . \quad (12)$$

Note that the values of η, β, and m for P-type and N-type are different (see Results section).

3. Short channel effects

It is well known that the threshold voltage changes as the device scales down due to several phenomena such as the charge sharing effect, the lateral non-uniform doping effect, and the Drain Induced Barrier Lowering (DIBL) effect [11]. The short channel effect at room temperature, which is effectively modelled in the BSIM model, is given by [14]

$$V_{th} = V_{th0} + \Delta Vth , \quad (13)$$

where

$$\Delta Vth = \Delta V_{LD} - \Delta V_{SC} - \Delta V_{DIBL} . \quad (14)$$

Here, ΔV_{LD} is the lateral non-uniform doping effect, ΔV_{SC} is the short channel effect, and ΔV_{DIBL} accounts for the DIBL effect (see [14] for detailed formula).

At low temperature, these effects are still present and must be modelled. For example, the charge sharing effect, which depends essentially on the depletion layer width, weakly varies when temperature down to 77 K [3] but it may strongly impact the threshold voltage once the substrate suffers strong freeze-out at very low temperaure [13]. For simplicity, we have devised an empirical function $f_{SC}(T)$ to fit the geometry effects on the threshold voltage over a wide temperature range:

$$f_{SC}(T) = \left(1 + sgn(\phi_F(T))\frac{\phi_F(T)}{\phi_F(T_c)}\right)\delta_{Vth} , \quad (15)$$

where ϕ_F is the Fermi potential (positive for PMOS - Eq. (11), negative for NMOS - Eq. (4)), and δ_{Vth} is a fitting parameter. T_C -the critical temperature (100 K), is empirically chosen at a point when the short channel effects are negligible. An extensive study on short channel effects at very low temperature is required to fully understand this phenomenon. Nevertheless, the presented fitting function Eq. (15) calculated from the proposed ϕ_F and the short channel effects at room temperature can predict the impact of short channel effects with temperature.

The threshold voltage with short channel effects is therefore given as

$$V_{th} = V_{th0} + \Delta Vth \times f_{SC}(T) . \quad (16)$$

4. Experimental setup

The NMOS and PMOS transistors used in this study were fabricated in the Austrian MicroSystems 0.35 μm CMOS (C35) p-substrate mixed signal process. The device geometries vary from 0.35 to 10 μm. The devices (64 transistors for each size)

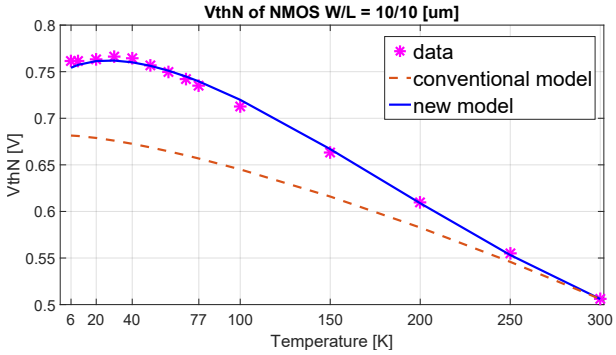

Figure 2: The temperature dependence of V_{th0} of NMOS: new model (Eq. (9)), conventional model (Eq. (1)) vs. experimental data (symbol)

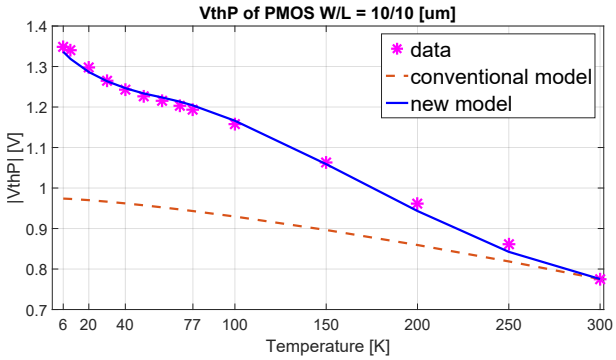

Figure 3: The temperature dependence of V_{th0} of PMOS: new model (Eq. (10)), conventional model (Eq. (1)) vs. experimental data (symbol)

were measured using a Keysight B1500A semiconductor analyzer with four Source Measurement Units (SMUs). The test chip was mounted in a Closed Cycle Refrigerator-based (CCR) cryogenic probe station (LakeShore CRX-4K) fitted with temperature controllers (LakeShore TC336). I-V curves were taken using pulsed measurement (duty cycle is 10% out of a 5 ms period) to minimize the self-heating effect. We used the Gm-Max method to extract the threshold voltage from Id-Vg measurements. This method eliminates the effect of series resistance which varies with temperature [4]. The mean value of the threshold voltage was taken from 64 extracted data with the maximum standard deviation is less than 10 mV.

5. Results and Discussions

The variation of the threshold voltage of a long channel NMOS as a function of temperature is shown in Fig. 2. The fitting parameter η in the Fermi potential model is 1.29, β = 10.365, and the freeze-out coefficient m in Eq. 7 is 1 over the 6-300 K temperature range. The other parameters such as T_{ox}, C_{ox}, ϕ_{gate}, Q'_o etc. are taken from AMS C35 process parameter [15] and calculated from extraction at room temperature. It is clear that the proposed model V_{th0} (Eq. 9) provides a better fit to the experimental data than the conventional model (Eq. 1) which is only valid at room temperatures.

The parameters η and β in the threshold voltage model for PMOS are 1.45 and 17.15, respectively. Unlike the NMOS, the

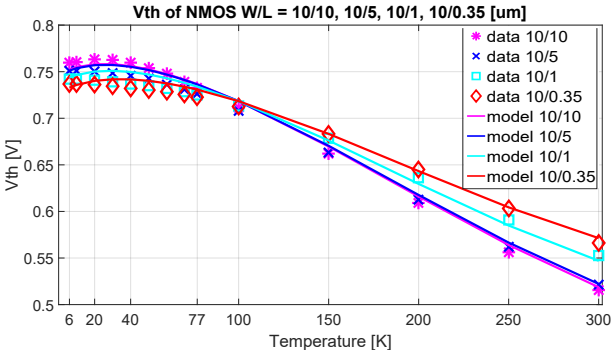

Figure 4: The short channel effects of NMOS V_{th}: model (–) vs. experimental data (symbol)

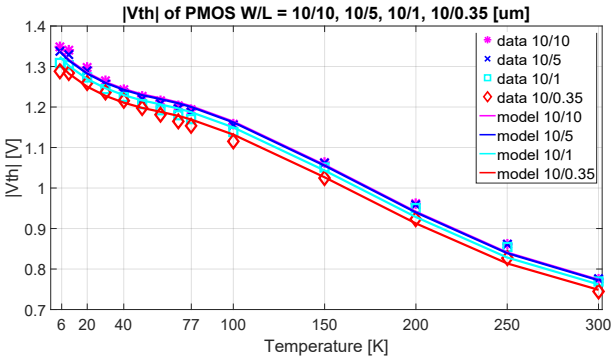

Figure 5: The short channel effects of PMOS V_{th}: model (–) vs. experimental data (symbol)

threshold voltage of PMOS does not saturate with decreasing temperature, rather it increases below 50 K as demonstrated in Fig. 3. The reason for this phenomenon could be due to the donors in P-channel suffer strong freeze-out. Consequently, further field-assisted ionization is required or the activation potential ϕ_{AF} must be greater at very low temperatures. To model this effect, the freeze-out coefficient m for PMOS (Eq. 12) is chosen as 0.9 for temperature below 50 K and 1.0 for above 50 K.

The V_{th} model of NMOS (δ_{Vth} = 4.3) and PMOS (δ_{Vth} = 0.075) with the short channel effects are depicted in Fig. 4 and Fig. 5, respectively. The data indicates that our equations model the temperature dependence of the threshold voltage for the long and short channel MOS over the 6–300 K temperature range. The maximum error between the proposed model and experiment is less than three percent.

6. Conclusion

We presented an enhanced threshold voltage model of NMOS and PMOS transistors for temperatures from 6 K to 300 K. The model is derived from the simplified Fermi potential which takes into account the carrier freeze-out effect. External field-assisted ionization is proposed and incorporated into the model to correct the threshold voltage. In addition, an empirical function that can be employed to estimate the short channel effects on the threshold voltage is also presented. The results from the proposed model demonstrate good agreement with data measured from fabricated chips. This model can also be adapted to fit with other technologies since it is derived from the physics of the bulk CMOS and process dependent parameters.

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