Modeling Triplet Spike Timing Dependent Plasticity Using Memristive Devices

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Keywords Memristor, synapse, spike, spike-timing-dependent plasticity (STDP).

Cite this article as:
Aghnout, S., Karimi, G. & Azghadi, M.R. J Comput Electron (2017). doi:10.1007/s10825-017-0972-0

Published version is available at:
https://link.springer.com/article/10.1007/s10825-017-0972-0

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Abstract Triplet-based Spike Timing Dependent Plasticity (TSTDP) is an advanced synaptic plasticity rule that results in improved learning capability compared to the conventional pair-based STDP (PSTDP). The TSTDP rule can reproduce the results of many electrophysiological experiments, where the PSTDP fails. This paper proposes a novel memristive circuit that implements the TSTDP rule. The proposed circuit is designed using three voltage (flux) driven memristors. Simulation results demonstrate that our memristive circuit induces synaptic weight changes that arise due to the timing differences among pairs and triplets of spikes. The presented memristive design is an initial step towards developing asynchronous TSTDP learning architectures using memristive devices. These architectures may facilitate the implementation of advanced large-scale neuromorphic systems with applications in real world engineering tasks such as pattern classification.

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1 Introduction

In 1971, Leon Chua introduced a new two-terminal circuit element, the memristor, as the fourth basic circuit component [1]. He suggested that the Hodgkin-Huxley membrane is a memristor and memristive devices can be used to fabricate synapses and neurons. The first realization of a physical memristor was reported by HP labs in 2008 [2].

Neuromorphic engineers have proposed various CMOS neuron circuitry which consume as very low electrical energy as the neurons in the brain [3-5]. However, each neuron in the brain may have up to ten thousands connections, called synapses, to its neighboring neurons. Therefore, designing low power dense synapses is quite critical in a neural network. Memristor is a very low power nano-scale device, which makes a perfect candidate for implementing synapses.

Spike Timing Dependent Plasticity (STDP) is the ability of synapses to modify their efficacy according to the time difference of pre- and post-synaptic spikes [6-8]. STDP learning in the brain is asynchronous and the synaptic weight change occurs while neurons communicate. In 2010, a memristor-based model for the spike-timing-dependent plasticity (STDP) was proposed [9-10], which considers a memristor as a synapse.

In addition to the classical pair-based STDP, triplet STDP has been shown to be another important property of the synapse [11–13]. In [11], Froemke and Dan's experiment on the triplet protocol in pyramidal neurons show that the synaptic modification is governed by three consecutive action potentials, instead of two. In 2006, Pfister and Gerstner demonstrated that the synaptic weight changes can be better explained considering time differences among triplets of spikes [12]. This is called triplet-based spike timing-dependent plasticity (TSTDP).

In a previous work a memristive design is developed to implement the STDP model presented by Froemke and Dan [11]. In addition, many other studies have implemented CMOS circuits representing the TSTDP rule [3, 5, 8]. However, to the best of our knowledge, no previous memristive implementation of TSTDP exists. In this paper, the TSTDP model is

realized in a memristive circuit. It is shown that the memristive model is compatible with both pair- and triplet-based STDP and is equivalent to the TSTDP model.
Here, we first review the synaptic plasticity rules in section 2. We then, in section 3, study a PSTDP memristive synapse model. Based on the TSTDP model by Pfister and Gerstner, we propose a memristive synapse circuit in section 4. In section 5, we compare our memristive circuit simulation results with the reported experimental data. Finally, we conclude the paper in section 6.

2 Synaptic Plasticity Rules

Synapses are inter-neuronal structures that allow chemical or electrical signals to transmit from pre- to target post-synaptic neuron with an associated efficacy. The synaptic weight or efficacy changes can be described by various equations called synaptic plasticity rules. These rules predict the synaptic weight modification as either depression or potentiation. Timing based synaptic plasticity rules, which consider the precise timing of pre and post-synaptic spikes, are reviewed in the following subsections.

2.1 Pair-Based STDP (PSTDP)

The classical form of STDP, known as the pair-based rule, has been studied widely and many VLSI implementations have been proposed so far [3, 14-15]. Eq. (1) is a mathematical representation of the original pair-based STDP rule [16],

$$\Delta w = \begin{cases} \Delta w^+ = A^+ e^{\left(\frac{-\Delta t}{\tau_+}\right)} & if \Delta t > 0 \\ \Delta w^- = -A^- e^{\left(\frac{\Delta t}{\tau_-}\right)} & if \Delta t \leq 0 \end{cases} \quad (1)$$

where $\Delta t = t_{post} - t_{pre}$ is the timing difference between a pair of pre- and post-synaptic spikes. Therefore, if a pre-synaptic spike arrives in a specified time window (τ_+) before a post-synaptic one, the synaptic weight will be potentiated. Vice versa, if a pre-synaptic spike occurs after the post-synaptic one, depression will occur. The amount of potentiation or depression is a function of the timing difference between pre- and post-synaptic spikes and the amplitude parameters, A^+ and A^-.

2.2 Triplet-Based STDP (TSTDP)

Many studies show that the traditional pair-based STDP is unable to reproduce the experimental results of various electrophysiological experiments like the data in [17] and [18]. Therefore, the TSTDP rule has been proposed to solve this problem.
In the TSTDP model, synaptic weight change is a function of the timing differences among a triplet set of spikes [12]. Eq. (2) is a mathematical representation of this learning rule, which has been proposed by Pfister and Gerstner in 2006 [12],

$$\Delta w = \begin{cases} \Delta w^+ = e^{\left(\frac{-\Delta t_1}{\tau_+}\right)}(A_2^+ + A_3^+ e^{\left(\frac{-\Delta t_2}{\tau_y}\right)}) \\ \Delta w^- = -e^{\left(\frac{\Delta t_1}{\tau_-}\right)}(A_2^- + A_3^- e^{\left(\frac{-\Delta t_3}{\tau_x}\right)}) \end{cases} \quad (2)$$

where $\Delta w = \Delta w^+$ for $t = t_{post}$ and $\Delta w = \Delta w^-$ for $t = t_{pre}$. Parameters A_2^+, $A2^-$, A_3^+ and A_3^- are potentiation and depression amplitude parameters, $\Delta t_1 = t_{post(n)} - t_{pre(m)}$, $\Delta t_2 = t_{post(n)} - t_{post(n-1)}$ and $\Delta t_3 = t_{pre(m)} - t_{pre(m-1)}$, are the time differences between combinations of pre- and post-synaptic spikes and finally τ_-, τ_+, τ_x and τ_y are time constants [12]. In our study, the proposed memristive circuit aims to simulate the model presented in Eq. (2).

3 Memristor as a Synapse: Modeling Pair-Based STDP

Defining a memristor (see Fig. 1(a)) as the fourth electrical element may have some ambiguities. Leon Chua considers a memristive device, or a memristor, as any element that has an *I(V)* curve pinched at *0 V* (Fig. 1(b)) [19].
In neuromorphic engineering domain, memristors are resistive components with the following properties: *i)* increase of the electrical charge passing through the

component decreases the resistance value, *ii)* decrease of the electrical charge passing through the component increases the resistance value and *iii)* the resistance value is non-volatile even after it is turned off. Moreover, the change of resistance appears if the memristor voltage goes beyond a 'threshold' (Fig. 1(c)).

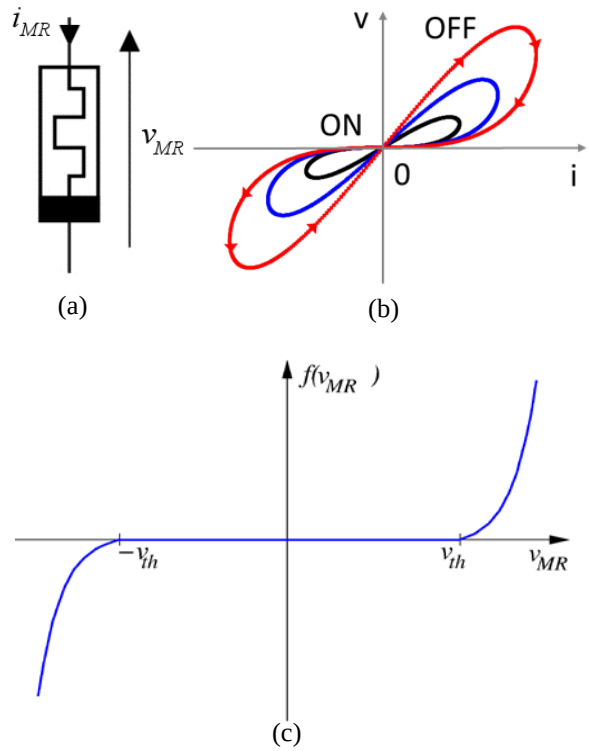


Fig. 1 a Memristor asymmetric symbol, **b** Memristor hysteresis curve pinching at origin, **c** Memristor non-linear weight update function with exponential growth and thresholding (figures are extracted from reference no [20])

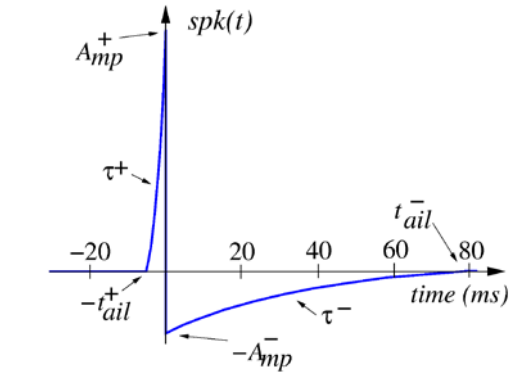
Based on an analogy between the non-volatility in the memristor and the long-term plasticity in the synaptic weight, the first fully asynchronous memristive synaptic model was established by Zamarreno-Ramos et al. [9]. In this model, a voltage/flux driven memristor with two thresholds is used as the synapse to model the PSTDP rule and the memristance (synaptic efficacy) is updated only if the memristor voltage exceeds the thresholds.
Here, the action potentials have a form of piecewise exponential function, as shown in Fig. 2 (a), which is in accordance with the actual spike shape and can be represented as

$$spk(t) = \begin{cases} A_{mp}^{+} \dfrac{e^{\frac{t}{\tau^{+}}} - e^{-\frac{t_{ail}^{+}}{\tau^{+}}}}{1 - e^{\frac{t_{ail}^{+}}{\tau^{+}}}} & if \ -t_{ail}^{+} < t < 0 \\ -A_{mp}^{-} \dfrac{e^{-\frac{t}{\tau^{-}}} - e^{-\frac{t_{ail}^{-}}{\tau^{-}}}}{1 - e^{\frac{t_{ail}^{-}}{\tau^{-}}}} & if \ 0 < t < t_{ail}^{-} \\ 0 & if \ otherwise \end{cases} \quad (3)$$

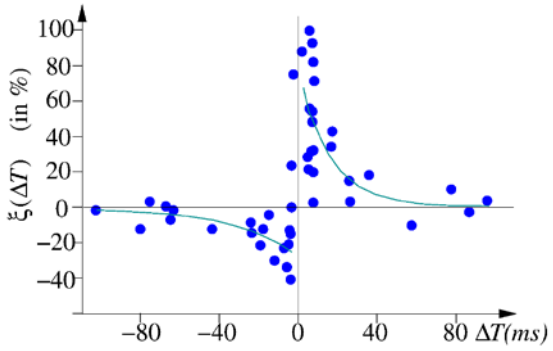
Axons and dendrites operate as transmission lines, so it is reasonable to expect some attenuation when the spikes arrive at the respective synapses [9]. Therefore, α_{pre} is supposed to be the attenuation for the pre-synaptic spike $V_{mem-pre}(t) = \alpha_{pre}\, spk(t + \Delta t)$, and α_{pos} for the post-synaptic spike $V_{mem-pos}(t) = \alpha_{pos} spk(t)$. Under these situations, memristor voltage is $V_{mem}(t,\Delta t) = \alpha_{pos}\, spk(t) - \alpha_{pre}\, spk(t + \Delta t)$ and its memristance changes in response to timing differences between pre- and post-synaptic spikes can replicate the STDP update function as shown in Fig. 2(b) and reported in [9].
The memristive model presented in [9] corresponds to the conventional pair-based model and is incompatible with the triplet STDP protocol. In the following sections, we will show how a memristor circuit can model the higher-order STDP behavior of a synapse.

4 Modeling TSTDP Using Memristors

The pair-based STDP rule can correctly approximate the pair-based synaptic plasticity data. However, it fails to reproduce the synaptic changes for spike triplets. A triplet of spikes, as assumed in the TSTDP model of Eq. 2, is a case of pre-post-pre or post-pre-post spikes. Each of these cases is composed of two pairs of spikes but experiments show that these two spike pairs do not contribute independently to synaptic change [11].



(a)



(b)

Fig. 2 a Action potential as a piecewise exponential function (figures are extracted from reference no [10]), **b** Schematic of spike-timing-dependent plasticity. The circles are experimental recordings and the solid curve is a fitting STDP function (figures are extracted from reference no [21])

The triplet-based spike timing-dependent plasticity (TSTDP) presented by Pfister & Gerstner (Eq. 2) [12], uses higher order temporal patterns of spikes to modify the synaptic weight and is compatible with the experimental results.

4.1 Modifying TSTDP Rule Equations

As seen in the array of equations shown in Eq. (2), each element of the array includes two components that are summed. The first component in both equations could be implemented using the memristive STDP model presented by Zamarreno-Ramos [9]. Using one memristor connecting pre and post neuron, the first part of the two equations in the array can be implemented. This memristor implements the effect of pairs of spikes. However, to realize the TSTDP rule, one should devise a method to implement the second parts of these equations, which include the effect of triplet of spikes.

In the case of post-pre-post, there is a pre synaptic spike, pre(m), and two post synaptic ones, post(n-1) and post(n). Therefore, the term $exp(-\Delta t_1/\tau_+)\times exp(-\Delta t_2/\tau_y)$ can be considered as the total weight change of a memristor whose memristance is updated in two steps. In the first step its weight change is proportional to $exp(-\Delta t_1/\tau_+)$ with $\Delta t_1 = t_{post(n)} - t_{pre(m)}$ and in the next step its weight change is proportional to $exp(-\Delta t_2/\tau_y)$ with $\Delta t_2 = t_{post(n)} - t_{post(n-1)}$. It will be shown that using a memristor and a few switches, these two steps can be implemented.

However, a challenge should be first addressed. Having the term $exp(-\Delta t_1/\tau_+)$, the weight has to be updated due to pre(m) and post(n) spikes and for the term $exp(-\Delta t_2/\tau_y)$, the weight should be altered due to post (n-1) and post(n) spikes. The problem arises here. The spikes pre(m) and post(n) come after each other and updating the memristance due to these signals is by applying them to the two ports of a memristor. On the contrary, post (n-1) and post(n) are not adjacent and another pre spike may occur between them. Therefore, implementing the term $exp(-\Delta t_2/\tau_y)$, where $\Delta t_2 = t_{post(n)} - t_{post(n-1)}$, is not straightforward. Therefore, the TSTDP equations should be changed to overcome this problem. The new equations could be written as:

$$A_3^+ exp\left(\frac{-(t_{post(n)}-t_{pre(m)})}{\tau_+}\right) exp\left(\frac{-(t_{post(n)}-t_{post(n-1)})}{\tau_y}\right) =$$
$$A_3^+ exp\left(\frac{-(t_{post(n)}-t_{pre(m)})}{\tau_+}\right) exp\left(\frac{-(t_{post(n)}-t_{pre(m)})}{\tau_y}\right)$$
$$exp\left(\frac{-(t_{pre(m)}-t_{post(n-1)})}{\tau_y}\right) =$$
$$A_3^+ exp\left(\frac{-(t_{post(n)}-t_{pre(m)})}{\tau}\right) exp\left(\frac{-(t_{pre(m)}-t_{post(n-1)})}{\tau_y}\right)$$
$$where\ \frac{1}{\tau} = \frac{1}{\tau_+} + \frac{1}{\tau_y} \qquad (4)$$

Now considering τ, the weight is updated in two steps. In the first step, the weight change equals $exp(-\Delta t_1/\tau)$ and is due to

spikes post(n) and pre(m), that are successive spikes. In the next updating step, the weight change is due to spikes post(n-1) and pre(m), which are also successive spikes. This is equal to $exp(-\Delta t_2/\tau_y)$, where $\Delta t_2 = t_{pre(m)} - t_{post(n-1)}$. Therefore, the memristive circuit is easier to implement. Introducing the new parameter τ, can be considered as an alteration to the TSTDP rule to make it compatible to memristive implementations.

As mentioned in [9] axons and dendrites of a neuron operate as transmission lines, so it is reasonable to expect some attenuation when the spikes arrive at the respective synapses. Here, α_{pre} is the attenuation coefficient for the pre-synaptic spike and α_{post} is the attenuation coefficient for the post-synaptic spike. Interestingly, by changing the pre or post synaptic attenuation coefficient, α_{pre} and α_{post}, the new parameter τ could be changed. A series of simulation was performed to clarify the impact of attenuation coefficients on τ. These simulations demonstrate that by decreasing α_{pre} and α_{post}, the coefficient τ also decreases, as shown in Fig. 3.

4.2 The Proposed Memristive Circuit

Considering the modified TSTDP equation (Eq. 4), three parallel memristors can be used to implement the TSTDP learning algorithm. It is known that when two or more memristors are in parallel with the same polarity, the total conductance is the sum of all conductances. Therefore, using three parallel memristors, all parts of the new triplet equations can be implemented and summed up. The first memristor similar to the Zamarreno-Ramos et al. model implements the first part of the equation, including the effect of pairs of spikes. The second memristor in combination with a few switches, implement the term $exp(-\Delta t_1/\tau)exp(-\Delta t_2/\tau_y)$. The third memristor also in combination with a few switches implement the triplet depression term $exp(\Delta t_1/\tau')exp(-\Delta t_3/\tau_x)$, where $\Delta t_3 = t_{post(n)} - t_{pre(m-1)}$. The proposed 3-memristor circuit is depicted in Fig. 4. In addition, Fig. 5 demonstrates synaptic weight changes for the case of post-pre-post triplet, while a similar approach applies for the pre-post-pre case.

The proposed memristive circuit shown in Fig. 4 works as follows: The first memristor Mem. 1, acts in the same way as the single memristor of Zamarreno-Ramos et al. model, which receives spikes directly from pre and post neurons and implements the effect of pairs of spikes. It accounts for the first parts of the two equations in the array of Eq. 2.

The second memristor, Mem. 2, implements the second part of the first equation in the array of Eq. 2, i.e. $exp(-(t_{post(n)}-t_{pre(m)})/\tau_+)exp(-(t_{post(n)}-t_{post(n-1)})/\tau_y)$. As shown in Eq. 4, this can be modified to $exp(-(t_{post(n)}-t_{pre(m)})/\tau)exp(-(t_{pre(m)}-t_{pos(n-1)})/\tau_y)$. As shown in Fig. 5, when a post-pre-post triplet occurs there will be two time intervals, the first one between $t_{post(n-1)}$ and $t_{pre(m)}$ and the second between $t_{pre(m)}$ and $t_{post(n)}$. In the first time interval, i.e. before pre(m) arrives, switches S1 and S2 are closed and S3 and S4 are open. Therefore, spike post(n-1) is applied to the positive port of Mem. 2, and spike pre(m) is applied to the negative port. Therefore, the synaptic weight of Mem. 2 experience a potentiation proportional to $exp(-(t_{pre(m)}-t_{post(n-1)})/\tau_y)$. In this time interval, Mem. 2 is disconnected from the rest of the circuit and its weight is being updated.

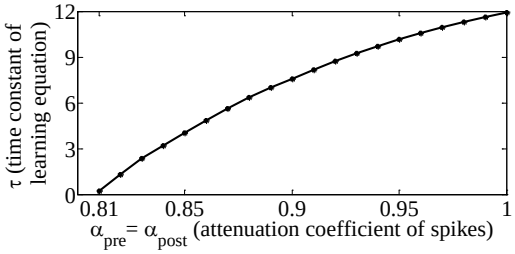


Fig. 3 Coefficient τ as a function of attenuation coefficient of pre and post spikes, α_{pre} and α_{post}.

In the second time interval, switches S1 and S2 are open and S3 and S4 are closed. Now, Mem. 2 is in the circuit and spike pre(m) is applied to the positive port of it

and spike post(n) is applied to its negative port. Therefore, the synaptic weight of Mem. 2 has a potentiation proportional to $exp(-(t_{post(n)}-t_{pre(m)})/\tau)$. So using these switches, the total weight change of Mem. 2 is proportional to $exp(-(t_{post(n)}-t_{pre(n)})/\tau)exp(-(t_{pre(n)}-t_{post(n-1)})/\tau_y)$.

When a pre-post-pre triplet occurs, a similar dynamic holds for Mem. 3 and its synaptic weight is updated in two time intervals. Therefore, the conductance of Mem. 3 updates in the first interval, while it is isolated from the rest of the circuit. In the second interval, Mem. 3 connects to the circuit and contributes with its updated weight. Therefore, the total weight change of Mem. 3 is proportional to $exp(t_{post(n)}-t_{pre(m)}/\tau')exp(-(t_{pre(m-1)}-t_{post(n)})/\tau_y)$.

Table 1 The proposed memristive circuit parameters (circuit in Fig. 4) for hippocampal data set. All voltages are normalized to the maximum spike amplitude (Amp^+ in Eq. 3)

	Memristor 1	Memristor 2	Memristor 3
Threshold Voltage (V_{th})	1.0841	0.9668	1.1115
$1/V_0$ (in Eq. 5 of [9])	6.9851	6.9454	7.0003
α_1 (attenuation coefficient of spike pre(n))	0.8974		
α_2 (attenuation coefficient of spike post(n))	0.9036		
α_3 (attenuation coefficient of spike pre(n))		0.8904	
α_4 (attenuation coefficient of spike post(n))		0.9296	
α_5 (attenuation coefficient of spike post(n-1))		0.8862	
α_6 (attenuation coefficient of spike pre(n))		0.9293	
α_7 (attenuation coefficient of spike pre(n))			0.9969
α_8 (attenuation coefficient of spike post(n))			0.9452
α_9 (attenuation coefficient of spike post(n))			0.9969
α_{10} (attenuation coefficient of spike pre(n-1))			0.9433

Table 2 The proposed memristive circuit parameters (circuit in Fig. 4) for visual cortex data set. All voltages are normalized to the maximum spike amplitude (Amp^+ in Eq. 3)

	Memristor 1	Memristor 2	Memristor 3
Threshold Voltage (V_{th})	1.1742	1.0008	0.9994
α_1 (attenuation coefficient of spike pre(n))	1		
α_2 (attenuation coefficient of spike post(n))	1		
α_3 (attenuation coefficient of spike pre(n))		1	
α_4 (attenuation coefficient of spike post(n))		0.9995	
α_5 (attenuation coefficient of spike post(n-1))		1	
α_6 (attenuation coefficient of spike pre(n))		0.9995	
α_7 (attenuation coefficient of spike pre(n))			0.9991
α_8 (attenuation coefficient of spike post(n))			0.9998
α_9 (attenuation coefficient of spike post(n))			0.9991
α_{10} (attenuation coefficient of spike pre(n-1))			0.9998

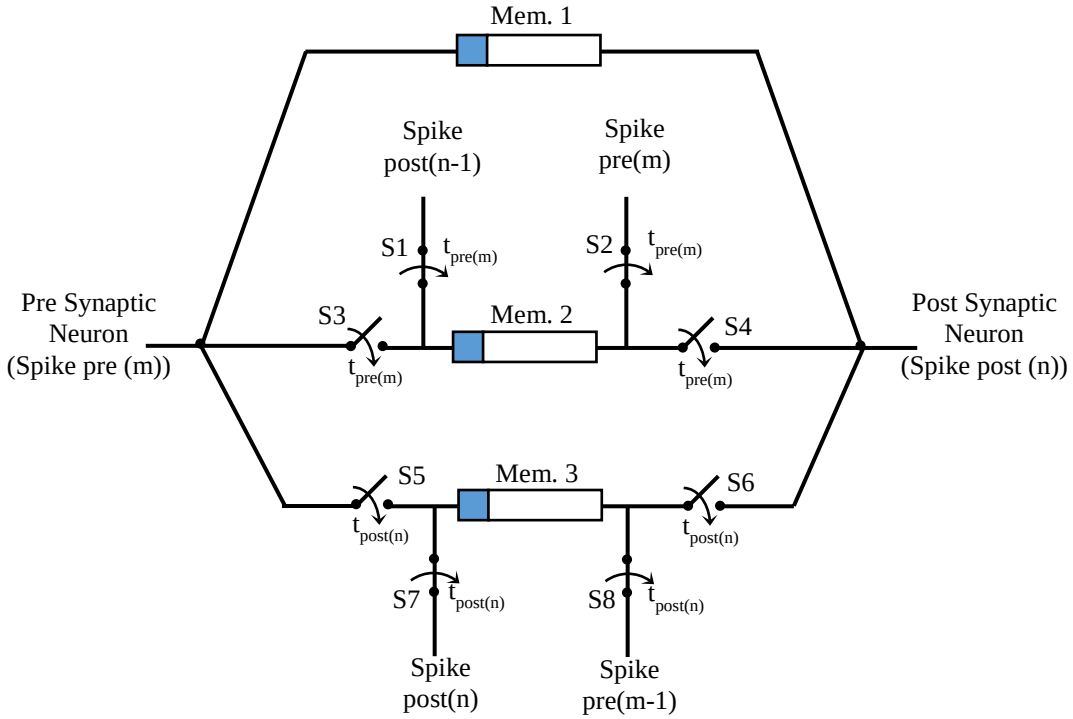


Fig. 4 Proposed memristive circuit

To verify the functionality of the proposed TSTDP circuit, different patterns of spikes like spike pairs and triplets were chosen. These spike patterns were applied to the circuit and resulted weight changes were compared to the experimental data. Different data sets, experimental protocols, data fitting method and the simulation results are explained in the following subsections.

5 Results

The proposed circuit shown in Fig. 4 was simulated in MATLAB using parameters in Tables 1 and 2. A normalized mean-square error similar to the one used in [12] has been used.

To verify the functionality of the proposed TSTDP circuit, different patterns of spikes like spike pairs and triplets were chosen. These spike patterns were applied to the circuit and resulted weight changes were compared to the experimental data. Different data sets, experimental protocols, data fitting method and simulation results are explained in the following subsections.

5.1 Data sets

The first data set utilized in this paper is composed of 10 data points, obtained from Table 1 of [12], and investigates how altering the repetition frequency of spike pairings affects the overall synaptic weight change (10 black data points and error bars shown in Fig. 7). The second experimental data set originates from hippocampal culture experiments [18], which examines pairing and triplet protocol effects on synaptic weight change. This data set consists of 10 data points obtained from Table 2 of [12] and shows the experimental weight change, Δw, as a function of the relative spike timing under pairing and triplet protocols in hippocampal culture.

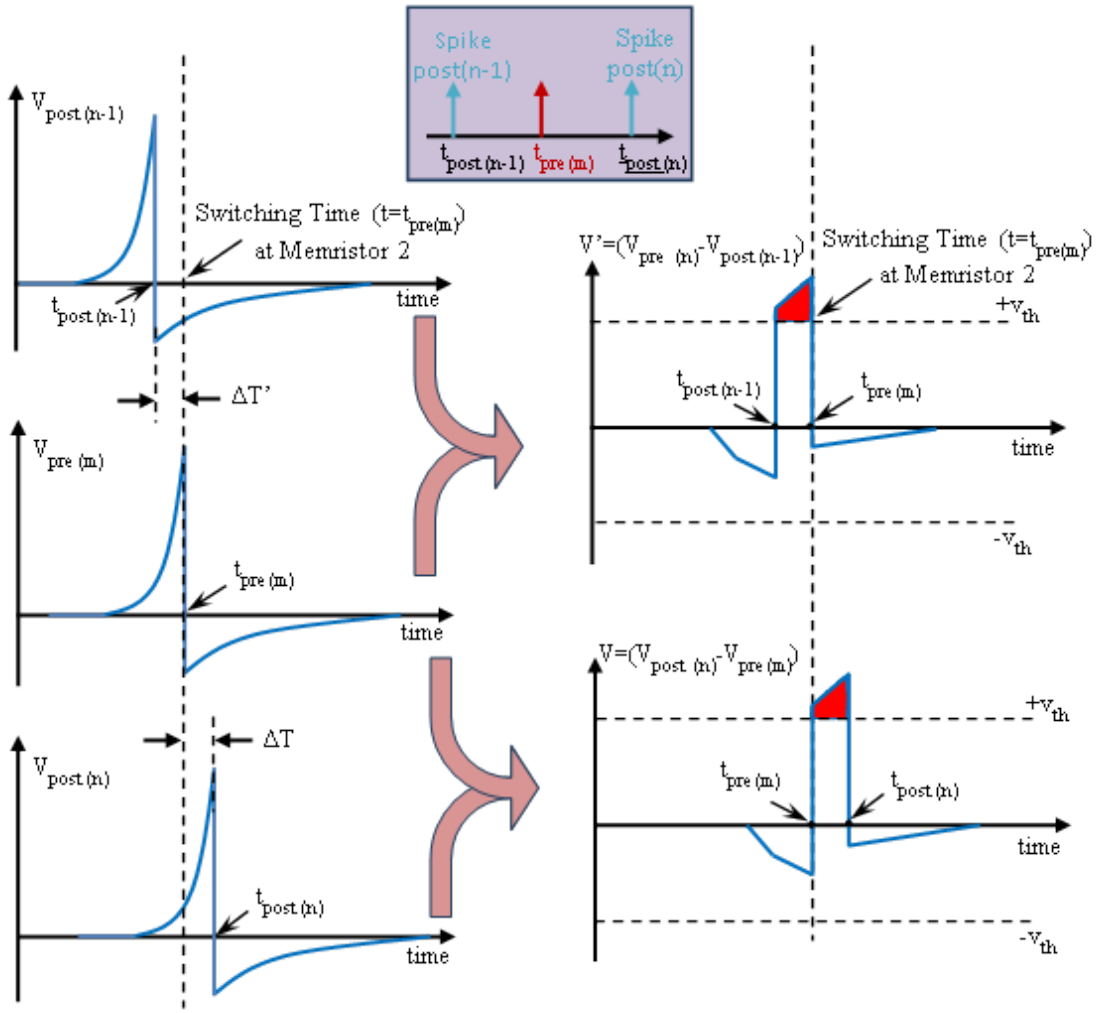


Fig. 5 The total memristance change of memristor 2 is updated in two steps. First step before t_{pre} and second step after t_{pre}.

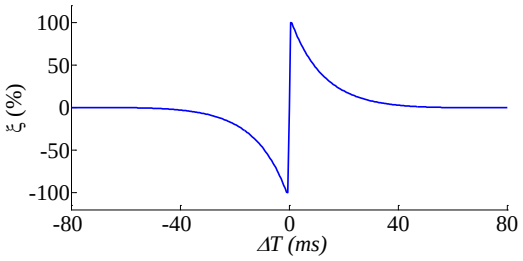


Fig. 6 Exponential learning window produced by the proposed TSTDP circuit and based on the pairing protocol.

5.2 Experimental protocols

5.2.1 Pairing protocol

The pair-based STDP protocol has been widely used in electrophysiological experiments and simulation studies. In this protocol, 60 pairs of pre- and post-synaptic spikes with a delay of $\Delta t = t_{post} - t_{pre}$ are used. Fig. 6 shows that the proposed circuit can reproduce the exponential learning window under the conventional pairing protocol described above and adopted in many experiments [18], [21]. This exponential learning window can also be reproduced using many PSTDP circuits.

However, biological experiments show that altering the spike pair repetition frequency affects the total synaptic weight change [17] and PSTDP circuits are not capable of reproducing this effect [22]. Here, Fig. 7 shows how the proposed TSTDP circuit can reproduce the effect of pairing repetition frequency.

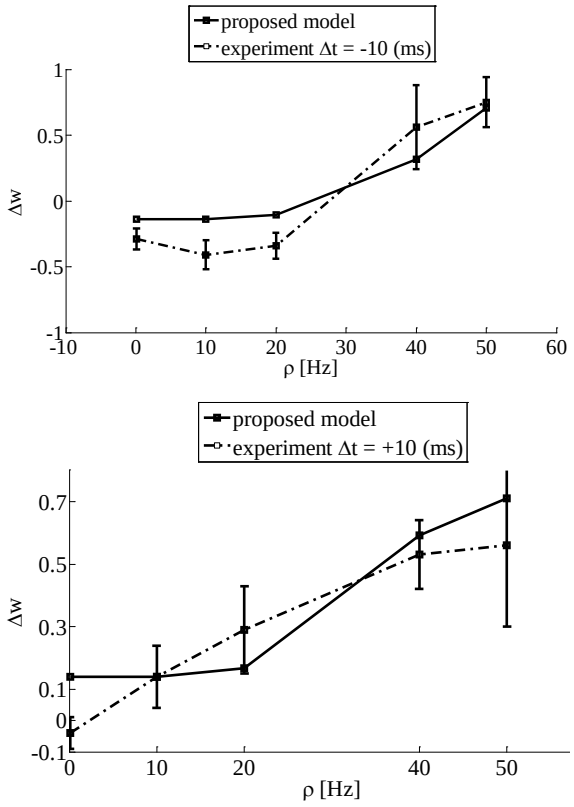


Fig. 7 Weight change in a pairing protocol as a function of the pairing frequency ρ reproduced by the proposed memristive TSTDP circuit. Experimental data points and error bars are extracted from [17]

5.2.2 Triplet protocol

In this and many other studies, two types of triplet patterns are used [12]. Both of them consist of 60 triplets of spikes, which are repeated at a given frequency of $\rho = 1$ *Hz*. The first one is a pre–post–pre pattern and there are two delays between the first pre and the middle post, $\Delta t_1 = t_{post(n)} - t_{pre(m-1)}$, and between the second pre and the middle post, $\Delta t_2 = t_{pre(m)} - t_{post(n)}$. The second pattern is a post–pre–post case where timing differences are defined as $\Delta t_1 = t_{pre(m)} - t_{post(n-1)}$ and $\Delta t_2 = t_{post(n)} - t_{pre(m)}$. Figs. 8 and 9 show how the proposed triplet circuit is in a close fit with the triplet experiments reported in Wang [18].

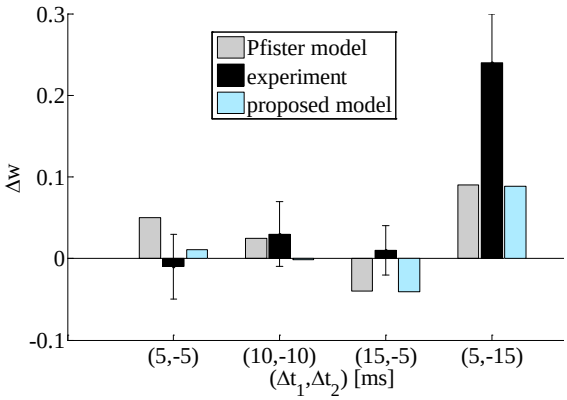


Fig. 8 Triplet protocol for the pre–post–pre combination of spikes produced by the proposed memristive TSTDP circuit. The experimental data corresponds to the hippocampal culture data [18]

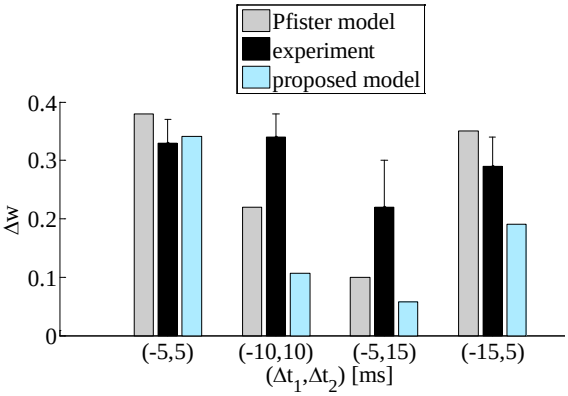


Fig. 9 Triplet protocol for the post–pre–post combination of spikes produced by the proposed memristive TSTDP circuit. The experimental data correspond to the hippocampal culture data set [18]

Table 3 Triplet protocol for the pre–post–pre combination of spikes (data from Fig. 8)

(Δt_1 , Δt_2)[ms] / Data sets	(5 , -5)	(10 , -10)	(15 , -5)	(5 , -15)
experimental data [18]	-0.01±0.04	0.03±0.04	0.01±0.03	0.24±0.06
model data [12]	0.05	0.025	-0.04	0.09
Proposed circuit	0.0107	-0.0016	-0.0410	0.0883

Table 4 Triplet protocol for the post–pre–post combination of spikes (data from Fig. 9)

(Δt_1 , Δt_2)[ms] / Data sets	(-5 , 5)	(-10 , 10)	(-5 , 15)	(-15 , 5)
experimental data [18]	0.33±0.04	0.34±0.04	0.22±0.08	0.29±0.05
model data [12]	0.38	0.22	0.1	0.35
Proposed circuit	0.3413	0.1072	0.0578	0.1910

Table 5 Average error between our proposed model and Pfister model with experimental date

	Average error between experimental data and TSTDP model (%)	Average error between experimental data and proposed circuit (%)
pre–post–pre case	54	40
post–pre–post case	15	35
total	**35**	**38**

Tables 3 and 4 summarize the data plotted in Figs. 8 and 9 and Table 5 shows the average error between TSTDP model [12] and experimental data [18], and between the proposed circuit model and experimental data [18]. There is 38% error between our proposed circuit and hippocampal culture data. This is an acceptable error compared to the error between the mathematical TSTDP model and hippocampal culture data of 35%, while the TSTDP model is our reference to implement the circuit. Therefore, the proposed memristive circuit can implement the TSTDP equations closely.

5.3 Data fitting approach

Identical to Pfister and Gerstner [12] that test their simulation results against the experimental data using a Normalized Mean Square Error (NMSE), the proposed circuit is verified by comparing its simulation results with the experimental data and capturing a small NMSE value. The NMSE is calculated using the following equation [12]:

$$NMSE = \frac{1}{p}\sum_{i=1}^{p}\left(\frac{\Delta w_{exp}^{i} - \Delta w_{cir}^{i}}{\sigma_i}\right)^2 \quad (5)$$

Where Δw_{exp}^{i} is the mean weight change obtained from biological experiments in [17], [18], Δw_{cir}^{i} is the weight change obtained from the proposed circuit, σ_i is the experimental standard error mean of Δw_{exp}^{i} for a given data point i and p is the number of data points in a specified data set.

In order to minimize the NMSE function and achieve the highest analogy to the experimental data, the normalized mean-square error of Eq. 5 has been minimized with MATLAB built-in function *lsqnonlin*. Therefore, the NMSE in Eq. 5 is written in an m-file as an error function. Then using the built-in function and starting from a

random point, this error function is minimized. In the starting point, the threshold voltage of all three memristors is set to 1 (all voltages are normalized to the spike amplitude A_{mp}^{+} in Eq. 3 and Fig. 2). Also, all ten attenuation coefficients are considered as 1 (each black line in Fig. 3 is a transmission line and has an attenuation coefficient) and parameter $1/V_0$ in Eq. 5 of [9] is set to 7. Starting from this point and solving a nonnegative least-square constraint problem, lsqnonlin function finds the minimum of the error function in Eq. 5. Table 1 and 2 demonstrates these sixteen circuit parameters achieved from the mentioned optimization method in order to reach the minimum NMSE for the two sets of data: the visual cortex data set and hippocampal culture data set. As shown in the previous section and Tables 3-5, using these adjusted parameters there is 38% error between the proposed circuit results and hippocampal culture data.

Using the optimized parameters, the final memristive circuit of Fig. 4 has been simulated in MATLAB and the error between the resulted Δw_{cir}^{i} and Δw_{exp}^{i} is plotted in Fig. 10. In each simulation, fifteen parameters are constant and the error is plotted versus the remaining ones. The value of adjusted circuit parameters which minimizes the Δw_{cir}^{i} error, obtained from Fig. 10, is almost the same as the values obtained from lsqnonlin function in Tables 1 and 2.

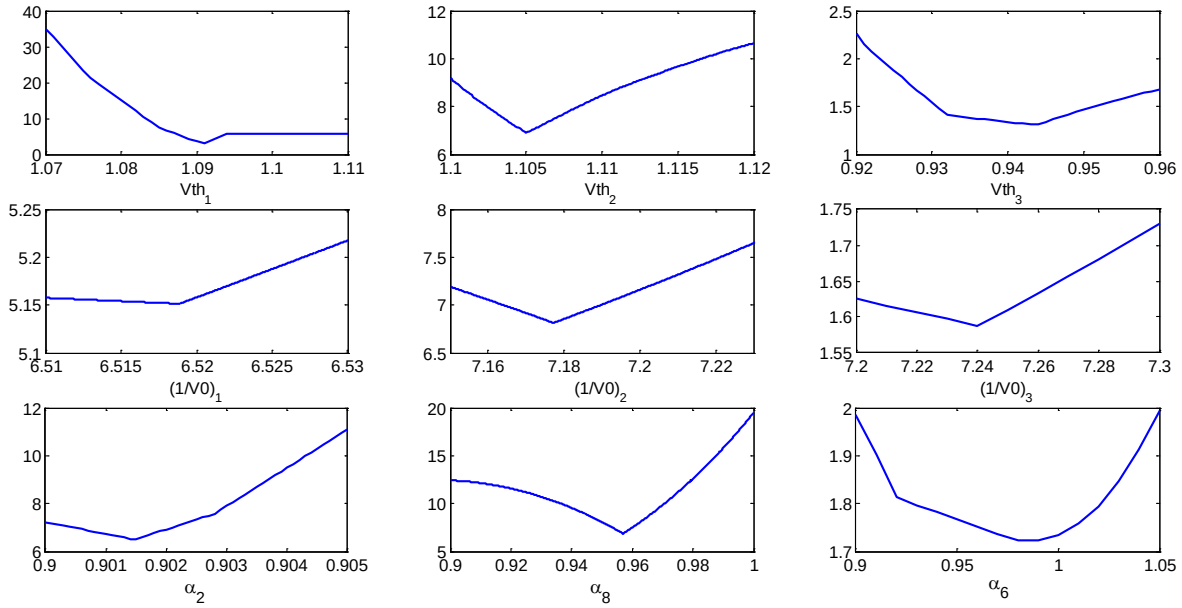


Fig. 10 The error between the resulted Δw_{cir}^{i} and Δw_{exp}^{i} as a function of circuit parameters (nine plots of sixteen are shown here). V_{th} of three memristors are normalized to spike amplitude A_{mp}^{+}

6 Discussion and conclusion

Biologically inspired chips have a long history since the work of Mead in 1989 [23] and are currently an interesting open area of research. These brain-like chips have many applications ranging from smart sensors to autonomous robotic systems. Therefore, a promising area of research is to use new technologies to translate biological setting into silicon chips. This translation currently faces many challenges including packaging density and adaptive connectivity between the processing centers of the chip.

Recently, many studies have introduced different design strategies for synaptic circuit, which update their efficacy according to some synaptic plasticity rules [14-15]. Most of previous works have focused on implementations of pair STDP.

In this work we have extended previous research and implemented a memristive triplet STDP circuit. We have shown that TSTDP learning rule can be induced by the voltage/flux driven formulation of a memristive circuit and a new triplet-based STDP circuit has been proposed.
The circuit was examined against various experimentally used induction protocols. It was shown that the proposed design is capable of demonstrating the exponential learning window of the PSTDP [21], the pairing frequency effect on the synaptic weight changes [17] and a similar synaptic behavior to different patterns of spike triplets [11-12], [18]. To the best of our knowledge, this is the first memristive circuit which is capable of reproducing all these experiments. This synapse can therefore be employed in future neuromorphic systems with high performance synaptic plasticity.

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